SONY

Diagonal 6.28 mm (Type 1/3) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX238LQJ-C

Description

The IMX238LQJ-C is a diagonal 6.28 mm (Type 1/3) CMOS active pixel type solid-state image sensor with a square pixel array and 1.37 M effective pixels. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, industrial cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Input frequency: 27 MHz / 54 MHz / 37.125 MHz / 74.25 MHz
- ◆Number of recommended recording pixels: 1280 (H) × 1024 (V) approx. 1.31 M pixels
- ◆Readout mode
  All-pixel scan mode
  720p-HD readout mode
  Vertical direction normal / inverted readout mode
  Horizontal direction normal / inverted readout mode
  Window cropping mode
- ◆Readout rate
  Maximum frame rate in all-pixel scan mode: 60 frame/s
- ◆Variable-speed shutter function (resolution 1H units)
- ◆12-bit A/D converter
- ◆CDS / PGA function
  -6 dB to 18 dB: Analog Gain (step pitch 0.3 dB)
  18.3 dB to 42 dB: Analog Gain 18 dB + Digital Gain 0.3 to 24 dB (step pitch 0.3 dB)
- ◆Supports I/O switching
  CMOS logic parallel SDR output
  Low voltage LVDS (150 m Vp-p) parallel DDR output
  Low voltage LVDS (150 m Vp-p) serial (1 ch / 2 ch / 4 ch switching) DDR output
- ◆Recommend lens F number: 2.8 or more
- ◆Recommended exit pupil distance: –30 mm to –∞

Exmor™
* “Exmor” is a trademark of Sony Corporation. The “Exmor” is a version of Sony's high performance CMOS image sensor with high-speed processing, low noise and low power dissipation by using column-parallel A/D conversion.

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Type 1/3
- ◆ Total number of pixels
  1312 (H) × 1069 (V) approx. 1.40 M pixels
- ◆ Number of effective pixels
  1305 (H) × 1049 (V) approx. 1.37 M pixels
- ◆ Number of active pixels
  1296 (H) × 1041 (V) approx. 1.35 M pixels
- ◆ Number of recommended recording pixels
  1280 (H) × 1024 (V) approx. 1.31 M pixels
- ◆ Chip size
  7.80 mm (H) × 7.50 mm (V)
- ◆ Unit cell size
  3.75 µm (H) × 3.75 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 4 pixels, rear 0 pixels
  Vertical (V) direction: Front 20 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 3 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 3.3 V)	AV_{DD}	-0.3	4.0	V	
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital 1.2 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	+75	˚C	
Storage temperature	Tstg	-30	+80	˚C	
Performance guarantee temperature	Tspec	-10	+60	˚C	

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	AV_{DD}	3.15	3.3	3.45	V
Supply voltage (interface 1.8 V)	OV_{DD}	1.7	1.8	1.9	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.1	1.2	1.3	V

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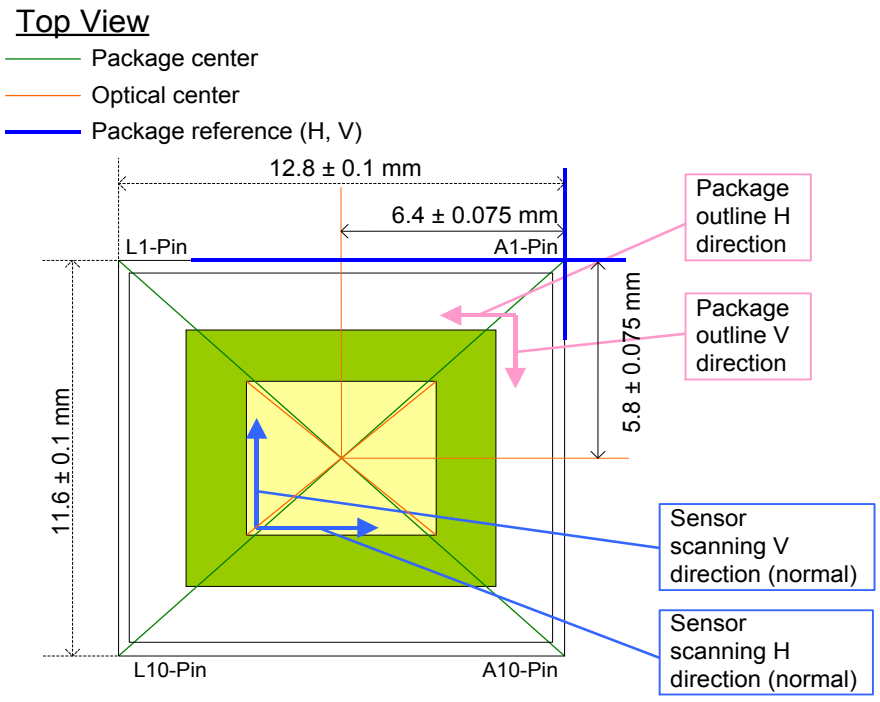
Contents

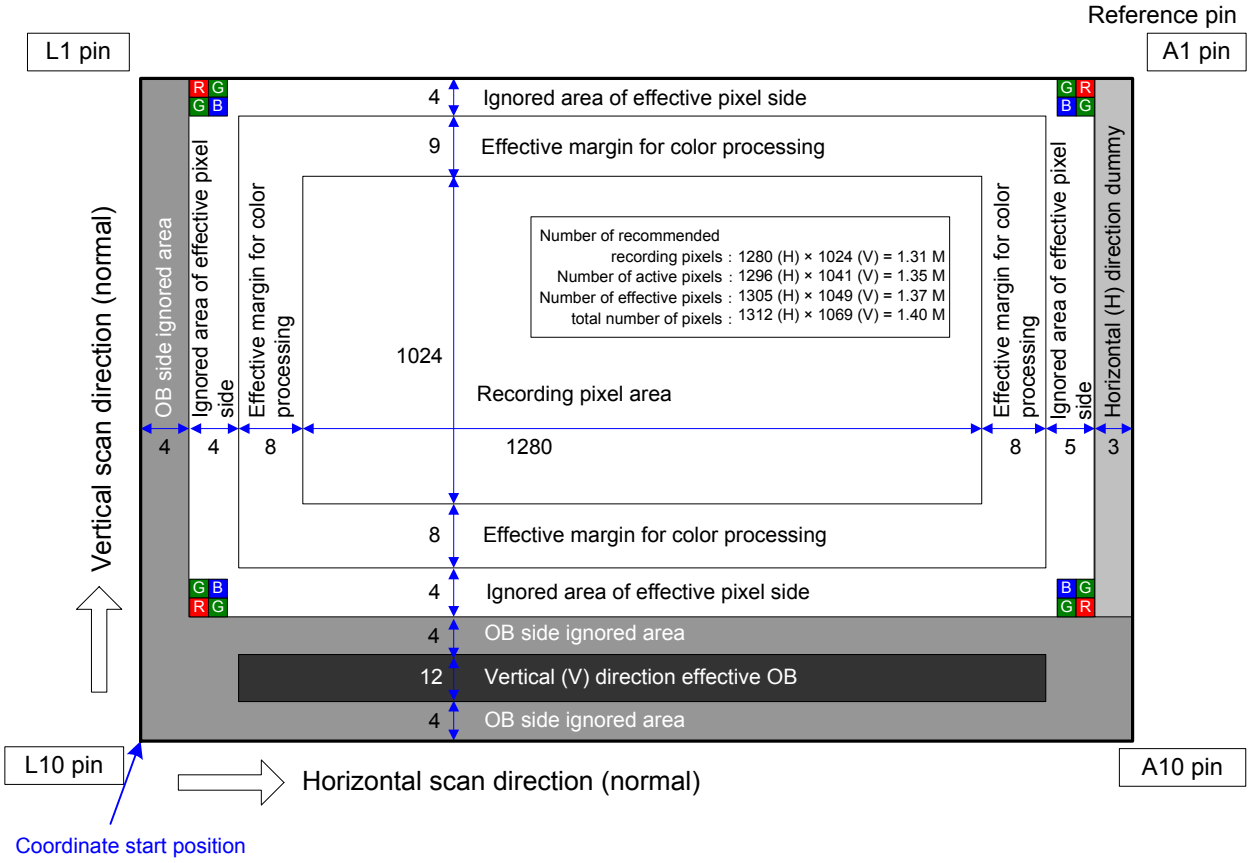
Chip Center and Optical Center



Optical Center

Pixel Arrangement

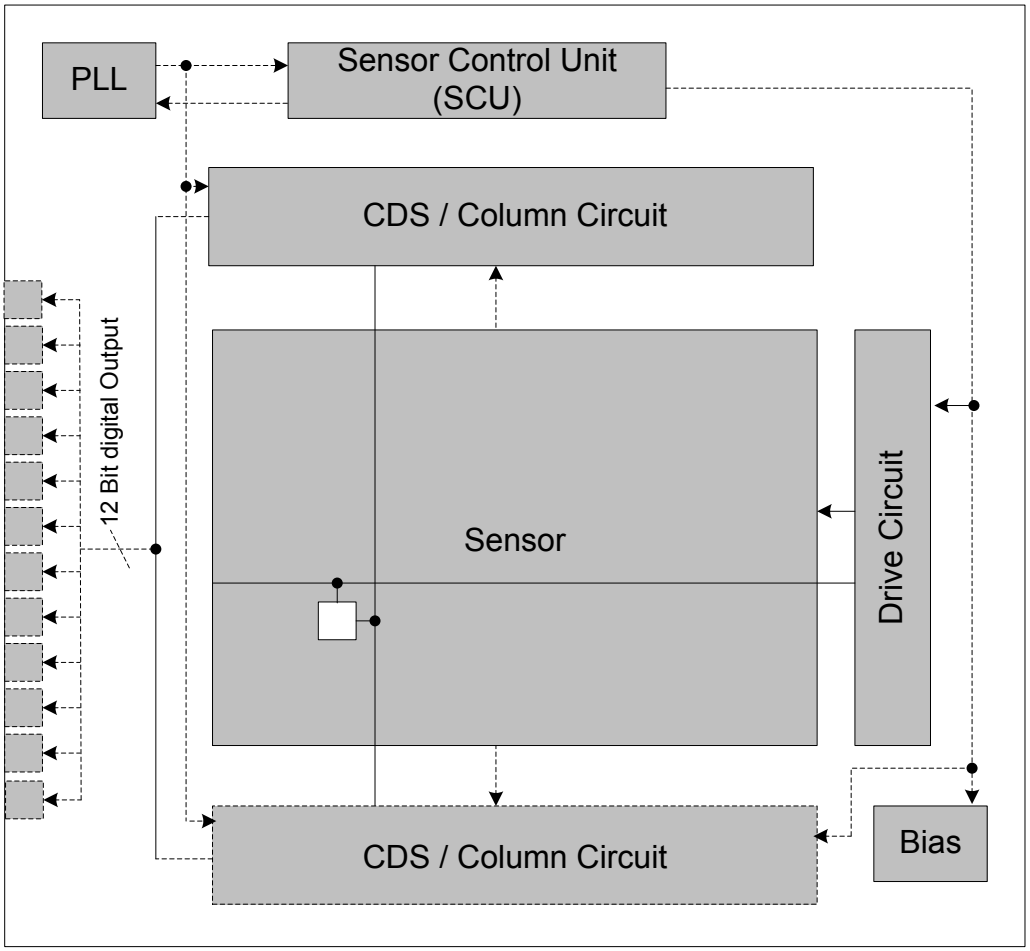
(Top View)



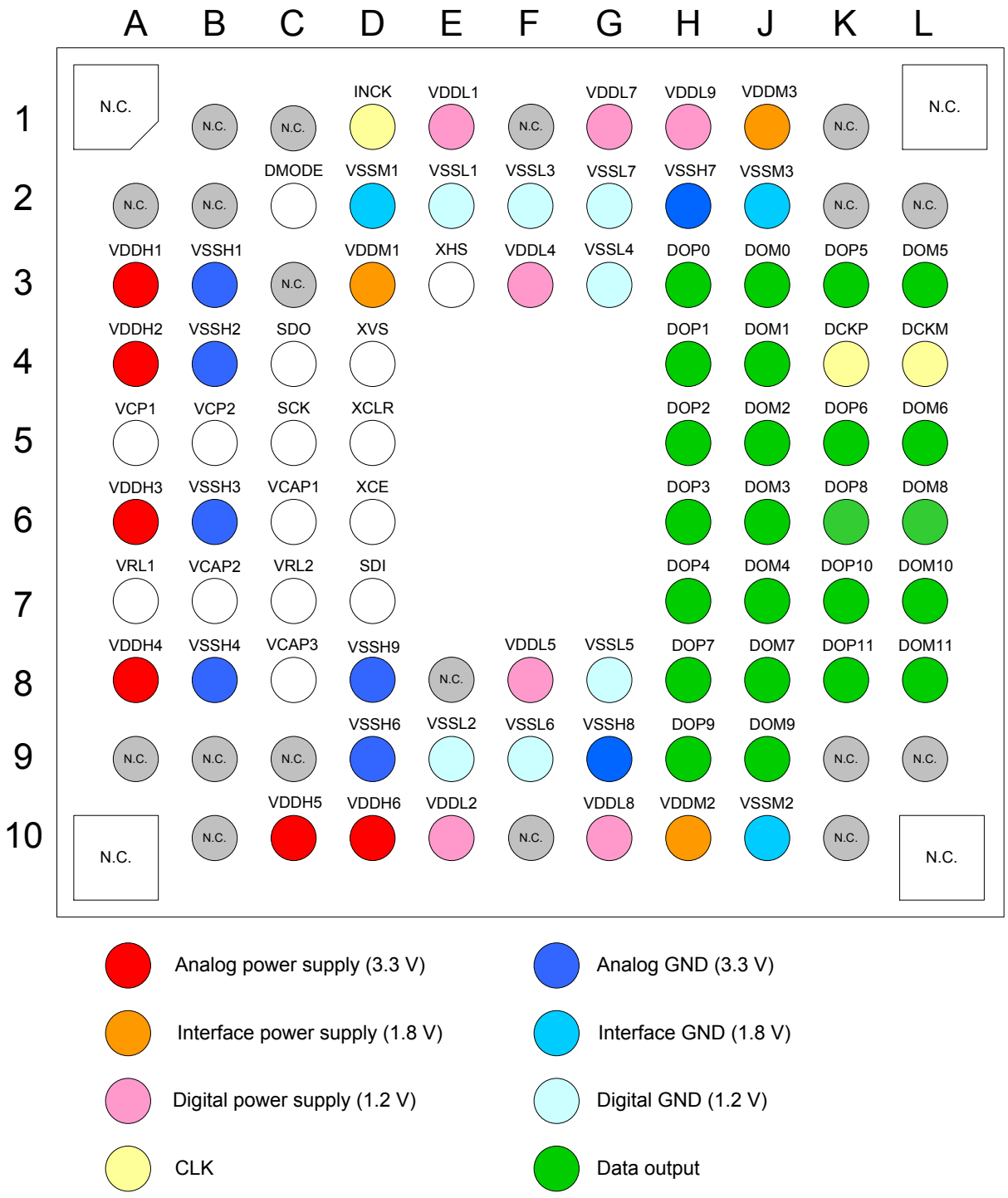
Pixel Arrangement

Block Diagram and Pin Configuration

(Top View)



Block Diagram



Pin Configuration (Bottom View)

Pin Description

No.	Pin No.	I/O	Analog / Digital	Symbol	Description	Remarks
1	A1	—	—	N.C.		
2	A2	—	—	N.C.		
3	A3	Power	A	VDDH1	3.3 V power supply	
4	A4	Power	A	VDDH2	3.3 V power supply	
5	A5	O	A	VCP1	Connected to VRL1 pin.	
6	A6	Power	A	VDDH3	3.3 V power supply	
7	A7	I	A	VRL1	Connected to VCP1 pin.	
8	A8	Power	A	VDDH4	3.3 V power supply	
9	A9	—	—	N.C.		
10	A10	—	—	N.C.		
11	B1	—	—	N.C.		
12	B2	—	—	N.C.		
13	B3	GND	A	VSSH1	3.3 V GND	
14	B4	GND	A	VSSH2	3.3 V GND	
15	B5	O	A	VCP2	Connected to VRL2 pin.	
16	B6	GND	A	VSSH3	3.3 V GND	
17	B7	O	A	VCAP2	Reference pin	
18	B8	GND	A	VSSH4	3.3 V GND	
19	B9	—	—	N.C.		
20	B10	—	—	N.C.		
21	C1	—	—	N.C.		
22	C2	I	D	DMODE	In slave mode: High / In master mode: Low	High = OV_{DD}, Low = GND
23	C3	—	—	N.C.		
24	C4	O	D	SDO	4-wire: Serial interface (Register value output) I^2C: OPEN	
25	C5	I	D	SCK / SCL	4-wire: Serial interface (Communication clock input) I^2C: Serial communication clock	
26	C6	O	A	VCAP1	Reference pin	
27	C7	I	A	VRL2	Connected to VCP2 pin.	
28	C8	O	A	VCAP3	Reference pin	
29	C9	—	—	N.C.		
30	C10	Power	A	VDDH5	3.3 V power supply	
31	D1	I	D	INCK	Master clock input	
32	D2	GND	D	VSSM1	1.8 V GND	
33	D3	Power	D	VDDM1	1.8 V power supply	
34	D4	I/O	D	XVS	Vertical Sync pulse	
35	D5	I	D	XCLR	System clear (Normal: High, Clear: Low)	High = OV_{DD}, Low = GND
36	D6	I	D	XCE	4-wire: Serial interface (Communication enable) I^2C: Fixed to High	High = OV_{DD}, Low = GND
37	D7	I	D	SDI / SDA	4-wire: Serial interface (Register value input) I^2C: Serial data input	
38	D8	GND	A	VSSH9	3.3 V GND	
39	D9	GND	A	VSSH6	3.3 V GND	
40	D10	Power	A	VDDH6	3.3 V power supply	

No.	Pin No.	I/O	Analog / Digital	Symbol	Description	Remarks
41	E1	Power	D	VDDL1	1.2 V power supply	
42	E2	GND	D	VSSL1	1.2 V GND	
43	E3	I/O	D	XHS	Horizontal Sync pulse	
44	E8	—	—	N.C.		
45	E9	GND	D	VSSL2	1.2 V GND	
46	E10	Power	D	VDDL2	1.2 V power supply	
47	F1	—	—	N.C.		
48	F2	GND	D	VSSL3	1.2 V GND	
49	F3	Power	D	VDDL4	1.2 V power supply	
50	F8	Power	D	VDDL5	1.2 V power supply	
51	F9	GND	D	VSSL6	1.2 V GND	
52	F10	—	—	N.C.		
53	G1	Power	D	VDDL7	1.2 V power supply	
54	G2	GND	D	VSSL7	1.2 V GND	
55	G3	GND	D	VSSL4	1.2 V GND	
56	G8	GND	D	VSSL5	1.2 V GND	
57	G9	GND	A	VSSH8	3.3 V GND	
58	G10	Power	D	VDDL8	1.2 V power supply	
59	H1	Power	D	VDDL9	1.2 V power supply	
60	H2	GND	A	VSSH7	3.3 V GND	
61	H3	O	D	DOP0	When CMOS parallel output: DO0 When Low voltage LVDS parallel output: DOP0 When Low voltage LVDS serial output: Hi-Z	
62	H4	O	D	DOP1	When CMOS parallel output: DO1 When Low voltage LVDS parallel output: DOP1 When Low voltage LVDS serial output: Hi-Z	
63	H5	O	D	DOP2	When CMOS parallel output: DO2 When Low voltage LVDS parallel output: DOP2 When Low voltage LVDS serial output: Hi-Z	
64	H6	O	D	DOP3	When CMOS parallel output: DO3 When Low voltage LVDS parallel output: DOP3 When Low voltage LVDS serial output: Hi-Z	
65	H7	O	D	DOP4	When CMOS parallel output: DO4 When Low voltage LVDS parallel output: DOP4 When Low voltage LVDS serial output: CHP2	
66	H8	O	D	DOP7	When CMOS parallel output: DO7 When Low voltage LVDS parallel output: DOP7 When Low voltage LVDS serial output: CHP3	
67	H9	O	D	DOP9	When CMOS parallel output: DO9 When Low voltage LVDS parallel output: DOP9 When Low voltage LVDS serial output: Hi-Z	
68	H10	Power	D	VDDM2	1.8 V power supply	
69	J1	Power	D	VDDM3	1.8 V power supply	
70	J2	GND	D	VSSM3	1.8 V GND	

No.	Pin No.	I/O	Analog / Digital	Symbol	Description	Remarks
71	J3	O	D	DOM0	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM0 When Low voltage LVDS serial output: Hi-Z	
72	J4	O	D	DOM1	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM1 When Low voltage LVDS serial output: Hi-Z	
73	J5	O	D	DOM2	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM2 When Low voltage LVDS serial output: Hi-Z	
74	J6	O	D	DOM3	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM3 When Low voltage LVDS serial output: Hi-Z	
75	J7	O	D	DOM4	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM4 When Low voltage LVDS serial output: CHM2	
76	J8	O	D	DOM7	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM7 When Low voltage LVDS serial output: CHM3	
77	J9	O	D	DOM9	When CMOS parallel output: Low output When Low voltage LVDS parallel output: DOM9 When Low voltage LVDS serial output: Hi-Z	
78	J10	GND	D	VSSM2	1.8 V GND	
79	K1	—	—	N.C.		
80	K2	—	—	N.C.		
81	K3	O	D	DOP5	When CMOS parallel output: DO5 When Low voltage LVDS parallel output: DOP5 When Low voltage LVDS serial output: CHP0	
82	K4	O	D	DCKP	When CMOS parallel output: DCK When Low voltage LVDS parallel output: DCKP When Low voltage LVDS serial output: DCKP	
83	K5	O	D	DOP6	When CMOS parallel output: DO6 When Low voltage LVDS parallel output: DOP6 When Low voltage LVDS serial output: CHP1	
84	K6	O	D	DOP8	When CMOS parallel output: DO8 When Low voltage LVDS parallel output: DOP8 When Low voltage LVDS serial output: Hi-Z	
85	K7	O	D	DOP10	When CMOS parallel output: DO10 When Low voltage LVDS parallel output: DOP10 When Low voltage LVDS serial output: Hi-Z	
86	K8	O	D	DOP11	When CMOS parallel output: DO11 When Low voltage LVDS parallel output: DOP11 When Low voltage LVDS serial output: Hi-Z	
87	K9	—	—	N.C.		
88	K10	—	—	N.C.		
89	L1	—	—	N.C.		
90	L2	—	—	N.C.		

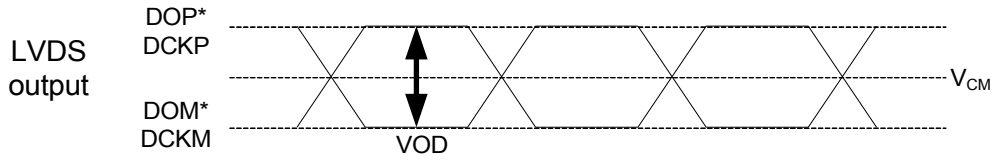
No.	Pin No.	I/O	Analog / Digital	Symbol	Description	Remarks
91	L3	O	D	DOM5	When CMOS parallel output: Low When Low voltage LVDS parallel output: DOM5 When Low voltage LVDS serial output: CHM0	
92	L4	O	D	DCKM	When CMOS parallel output: Low When Low voltage LVDS parallel output: DCKM When Low voltage LVDS serial output: DCKM	
93	L5	O	D	DOM6	When CMOS parallel output: Low When Low voltage LVDS parallel output: DOM6 When Low voltage LVDS serial output: CHM1	
94	L6	O	D	DOM8	When CMOS parallel output: Low When Low voltage LVDS parallel output: DOM8 When Low voltage LVDS serial output: Hi-Z	
95	L7	O	D	DOM10	When CMOS parallel output: Low When Low voltage LVDS parallel output: DOM10 When Low voltage LVDS serial output: Hi-Z	
96	L8	O	D	DOM11	When CMOS parallel output: Low When Low voltage LVDS parallel output: DOM11 When Low voltage LVDS serial output: Hi-Z	
97	L9	—	—	N.C.		
98	L10	—	—	N.C.		

* N.C. pins in the table above should be left open on the board.

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}		3.15	3.30	3.45	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK DMODE SCK SDI XCE	VIH	XVS / XHS in slave mode	0.8 OV_{DD}	—	—	V
			VIL		—	—	0.2OV_{DD}	V
Digital output voltage		DOP [11:0] DOM [11:0] DCKP DCKM	VOH	IOH = -2 mA	OV_{DD} -0.4	—	—	V
			VOL	IOL = 2 mA	—	—	0.4	V
			VCM	Low voltage LVDS	—	OV_{DD}/2	—	V
			VOD	Low voltage LVDS (Termination resistance100 Ω)	100	150	200	mV
		XHS XVS SDO	VOH	XVS / XHS In master mode	OV_{DD} -0.4			V
			VOL				0.4	V



Power Consumption

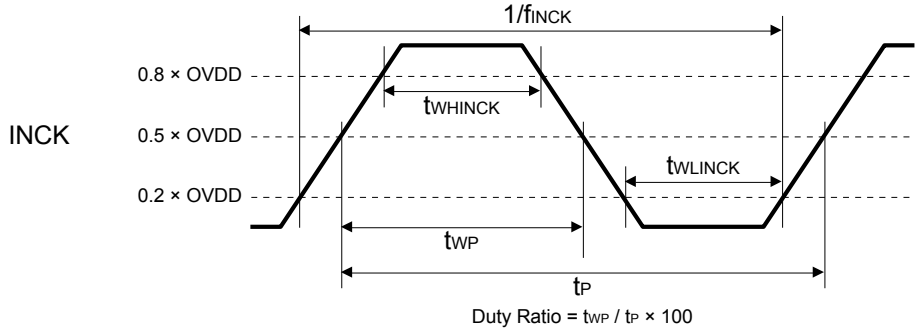
Item	Pins	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current Low-voltage LVDS parallel output 12 bit 60 frame/s All-pixel readout mode	VDDH	IAV_{DD}	61	61	90	90	mA
	VDDM	IOV_{DD}	22	20	34	34	mA
	VDDL	IDV_{DD}	61	77	90	111	mA
Operating current Low-voltage LVDS serial 4 ch output 12 bit 60 frame/s All-pixel readout mode	VDDH	IAV_{DD}	61	61	90	90	mA
	VDDM	IOV_{DD}	9	9	17	17	mA
	VDDL	IDV_{DD}	58	74	90	112	mA
Operating current CMOS parallel output 12 bit 60 frame/s 720p-HD mode	VDDH	IAV_{DD}	61	61	90	90	mA
	VDDM	IOV_{DD}	19	5	85	10	mA
	VDDL	IDV_{DD}	48	60	90	111	mA
Standby current	VDDH	IAV_{DD}_STB	—		0.2		mA
	VDDM	IOV_{DD}_STB	—		0.01		mA
	VDDL	IDV_{DD}_STB	—		6.2		mA

Operating current:
(Typical value condition): Supply voltage 3.3 V / 1.8 V / 1.2 V, 1/3 quantity of light of saturation, Tj = 25 ˚C
(Maximum value condition): Supply voltage 3.45 V / 1.9 V / 1.3 V, worst state of internal circuit operating current consumption, Tj = 60 ˚C
Standby (Maximum value condition): Supply voltage 3.45 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK = 0 V

Standard luminous intensity: luminous intensity at standard imaging condition I
Saturated luminous intensity: luminous intensity when the sensor is saturated.

AC Characteristics

Master Clock Waveform Diagram

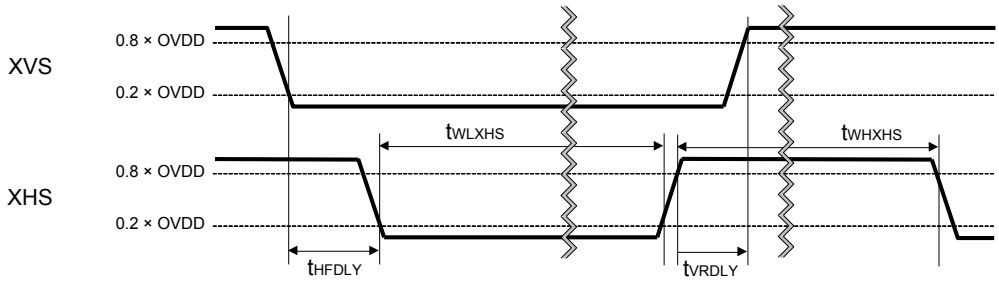


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK Low level width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK High level width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 27 MHz, 54 MHz, 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

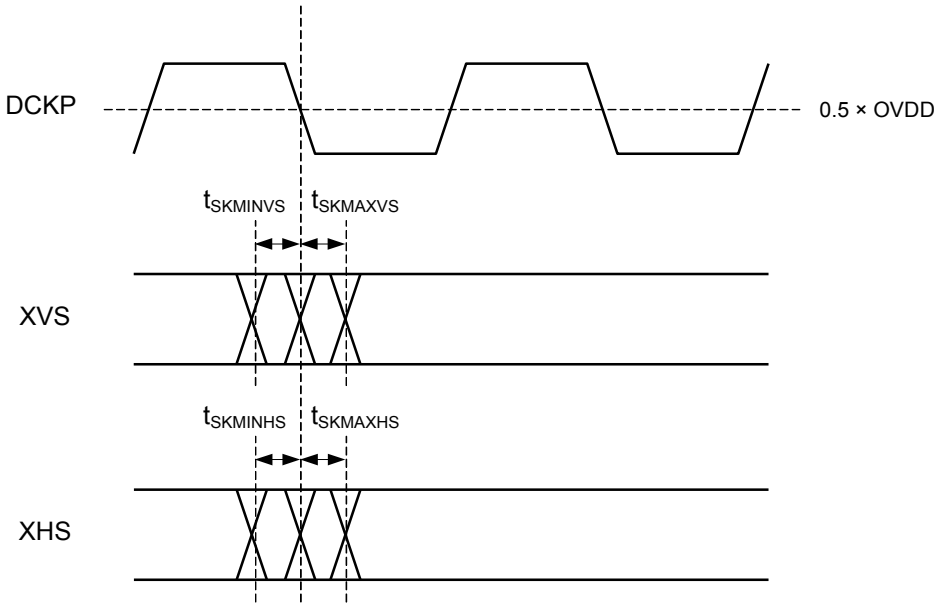
* The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (DMODE pin = High)



Item	Symbol	Min.	Typ.	Max.	Unit	Item
XHS Low level pulse width	t_{WLXHS}	$4/f_{INCK}$	—	—	ns	
XHS High level pulse width	t_{WHXHS}	$4/f_{INCK}$	—	—	ns	
XVS-XHS fall width	t_{HFDLY}	$1/f_{INCK}$	—	—	ns	
XHS-XVS rise width	t_{VRDLY}	$1/f_{INCK}$	—	—	ns	

XVS / XHS Output Characteristics In Master Mode (DMODE pin = Low, CMOS Output)

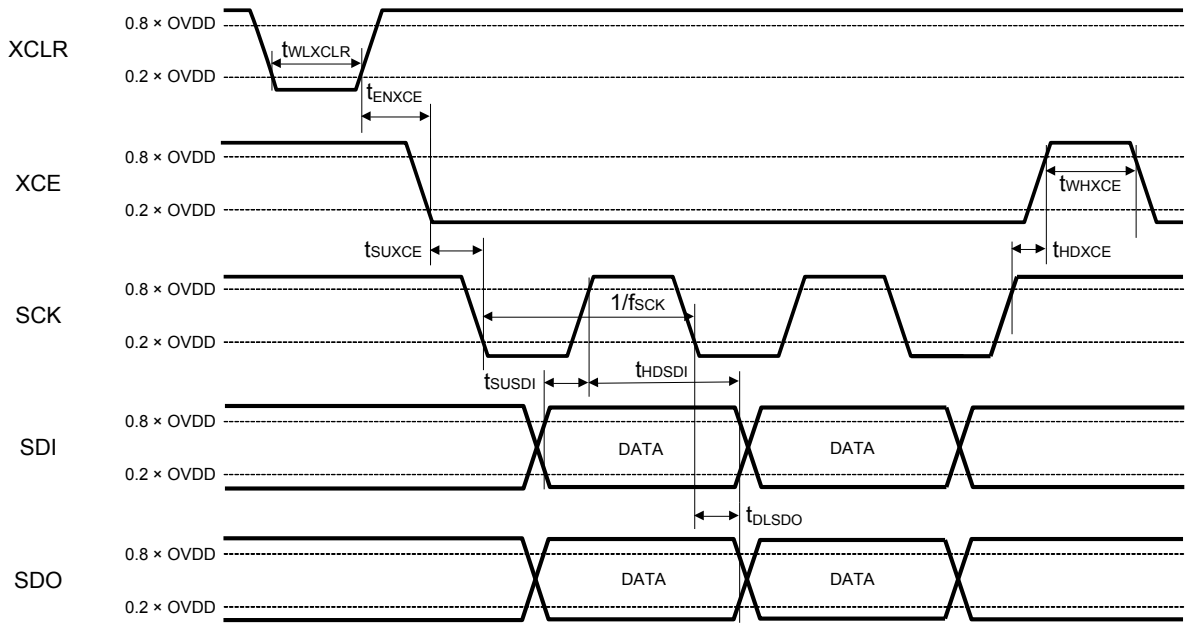


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCK - XVS skew Max.	$t_{SKMAXXVS}$	—	—	8	ns	Output load capacitance: 20 pF
DCK - XVS skew Min.	$t_{SKMINXVS}$	—	—	0	ns	Output load capacitance: 20 pF
DCK - XHS skew Max.	$t_{SKMAXXHS}$	—	—	8	ns	Output load capacitance: 20 pF
DCK - XHS skew Min.	$t_{SKMINXHS}$	—	—	0	ns	Output load capacitance: 20 pF

* XVS and XHS cannot be used for the sync signal to pixels.
  Be sure to detect sync code to detect the start of effective pixels in 1 line.

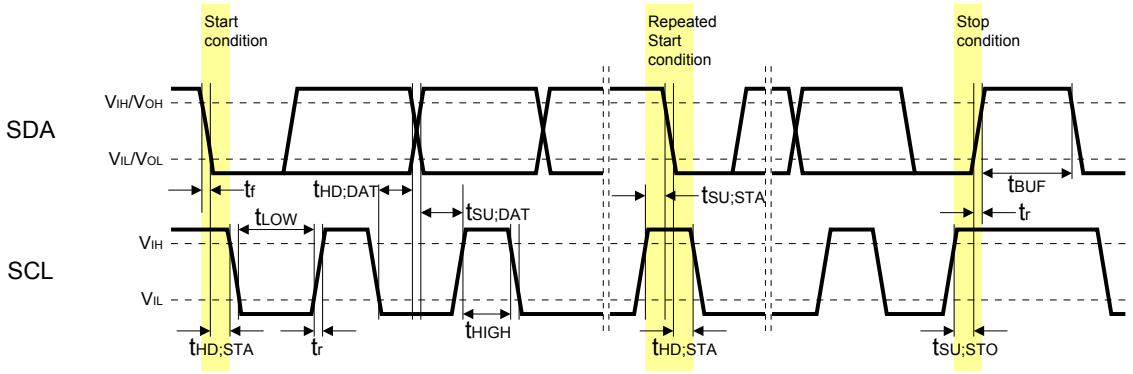
Serial Communication

4-wire



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK clock frequency	f_{SCK}	—	—	13.5	MHz	
XCLR Low level width	t_{WLXCLR}	$4/f_{INCK}$	—	—	ns	
XCE effective margin	t_{ENXCE}	20	—	—	µs	
XCE input setup time	t_{SUXCE}	20	—	—	ns	
XCE input hold time	t_{HDXCE}	20	—	—	ns	
XCE High level width	t_{WHXCE}	20			ns	
SDI input setup time	t_{SUSDI}	10	—	—	ns	
SDI input hold time	t_{HDSDI}	10	—	—	ns	
SDO output delay time	t_{DLSDO}	0	—	25	ns	Output load capacitance: 20 pF

I²C



I²C Specification

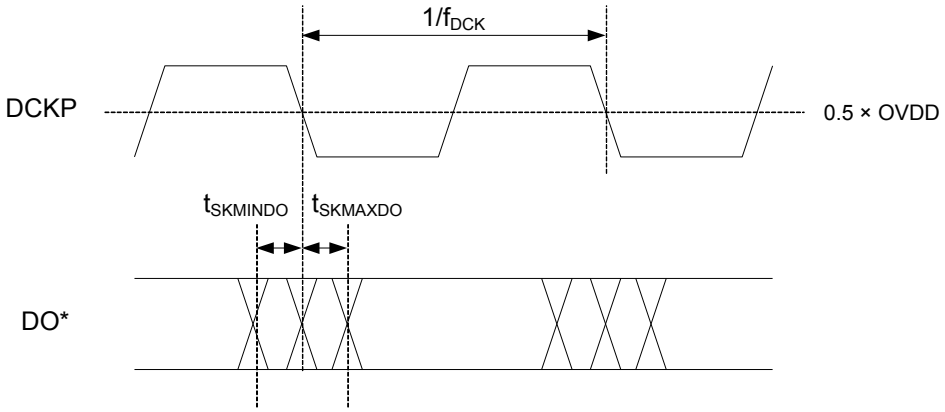
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OV_{DD} < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Capacitance for SCK (SCL) / SDI (SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	t_{HDSTA}	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	t_{SUSTA}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	0.9	µs
Data set-up time	t_{SUDAT}	100	—	—	ns
Rise time of both SDA and SCL signals	t_R	—	—	300	ns
Fall time of both SDA and SCL signals	t_F	—	—	300	ns
Set-up time (Stop Condition)	t_{SUSTO}	0.6	—	—	µs
Bus free time between a Stop and Start Condition	t_{BUF}	1.3	—	—	µs

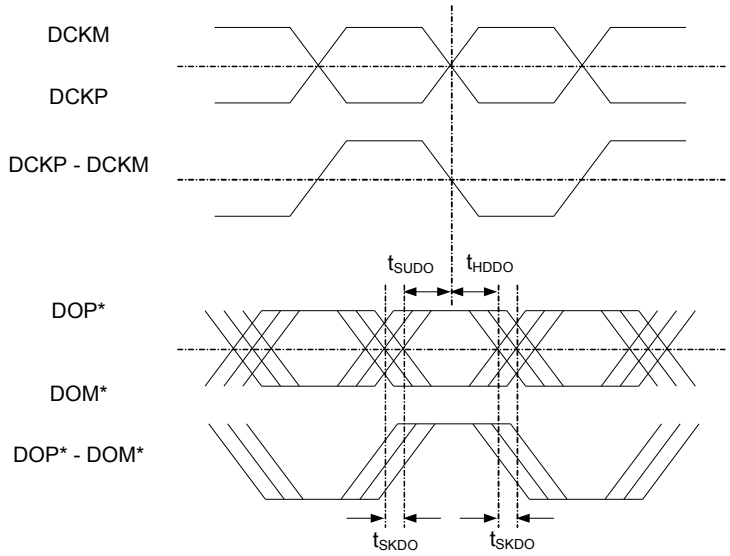
DCKP / DCKM, DOP / DOM

CMOS Outputs



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCK frequency	f_{DCK}	—	—	74.25	MHz	
DCKP clock duty	—	40	50	60	%	
DCK – DO skew max.	$t_{SKMAXDO}$	—	—	2	ns	Output load capacitance: 20 pF
DCK – DO skew min.	$t_{SKMINDO}$	—	—	2	ns	Output load capacitance: 20 pF

Low Voltage LVDS DDR Output



Parallel Output

(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCKP clock duty	—	45	50	55	%	DCK = 74.25 MHz (Max.)
DO skew time	t_{SKDO}	—	—	550	ps	Data Rate 74.25 MHz DDR
DO setup time	t_{SUDO}	800	—	—	ps	Data Rate 74.25 MHz DDR
DO hold time	t_{HDDO}	800	—	—	ps	Data Rate 74.25 MHz DDR

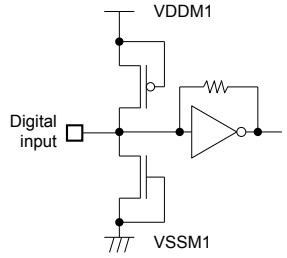
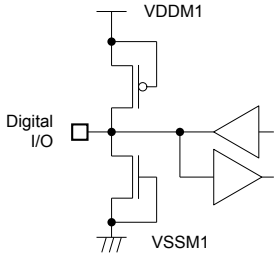
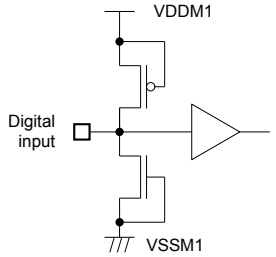
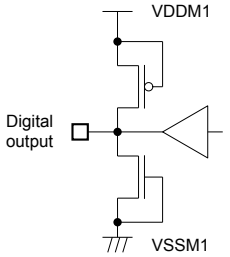
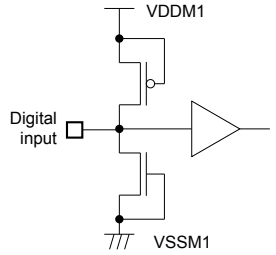
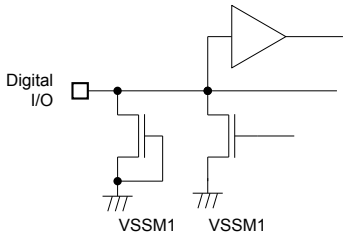
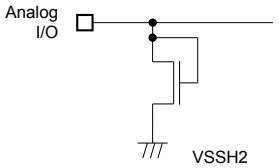
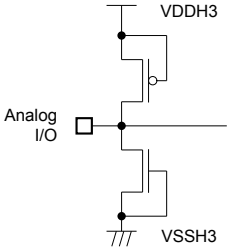
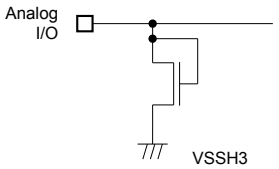
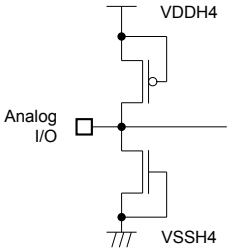
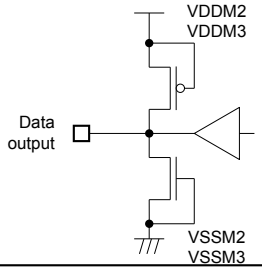
Serial Output

(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCKP clock duty	—	40	50	60	%	DCK = 297 MHz (Max.)
DO skew time	t_{SKDO}	—	—	400	ps	Data Rate 297 MHz DDR
DO setup time	t_{SUDO}	400	—-	—	ps	Data Rate 297 MHz DDR
DO hold time	t_{HDDO}	400	—	—	ps	Data Rate 297 MHz DDR

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS XHS	
XCLR		SDO	
DMODE XCE		SDI SCK	
VCP1 VCP2		VCAP1 VCAP2	
VRL1 VRL2		VCAP3	
DOPx DOMx DCKP DCKM			

Spectral Sensitivity Characteristics (TBD)

Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode 12 bit 30 frame/s, Gain = -6 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	TBD (TBD)	TBD (TBD)	—	Digit (mV)	1	1/30 s storage 12-bit output
Sensitivity ratio	R/G	RG	TBD	—	TBD		2	
	B/G	BG	TBD	—	TBD			
Saturation signal		Vsat01	TBD (TBD)	—	—	Digit (mV)	3	Zone0, Ⅰ 12-bit output
		Vsat2D	TBD (TBD)	—	—	Digit (mV)		Zone0 to Ⅱ' 12-bit output
Video signal shading		SH01	—	—	TBD	%	4	Zone0, Ⅰ
		SH2D	—	—	TBD	%		Zone0 to Ⅱ'
Dark signal		Vdt	—	—	TBD (TBD)	Digit (mV)	5	1/30 s storage 12-bit output
Dark signal shading		ΔVdt	—	—	TBD (TBD)	Digit (mV)	6	1/30 s storage 12-bit output
Line crawl R		Lcr	—	—	TBD	%	7	
Line crawl B		Lcb	—	—	TBD	%		
Lag		Lag	—	—	TBD	%	8	

Note) 1. Converted value into mV using 1Digit = 0.373 mV for 12-bit output.
2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the glass.

Video Shading Zone Definition

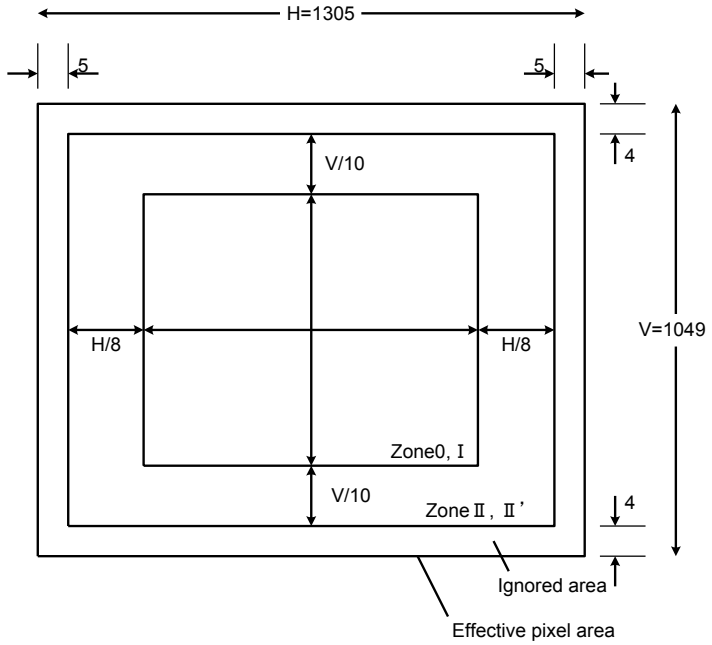


Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr / Gb channel signal output or the R / B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100/30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to TBD mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, TBD mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is TBD mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / TBD × 100 [%]

5. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

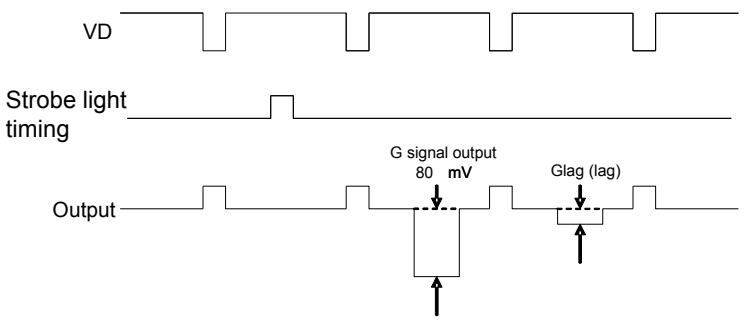
   ΔVdt = Vdmax – Vdmin [mV]

7. Line crawl
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr signal output to TBD mV, insert R and B filters and measure the difference between G signal lines (ΔGlr, ΔGlb [mV]) as well as the average values of the G signal outputs (Gar, Gab). Substitute the values into the following formula.

   Lci = (ΔGli / Gai) × 100 [%] (i = r, b)

8. Lag
   Adjust the G signal output value generated by strobe light to 80 mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Glag), and substitute the value into the following formula.

   Lag = (Glag / 80) × 100 [%]



Setting Registers with Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^2C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^2C communication is shared, so the external pin XCE must be fixed to power supply side when using I^2C communication.

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

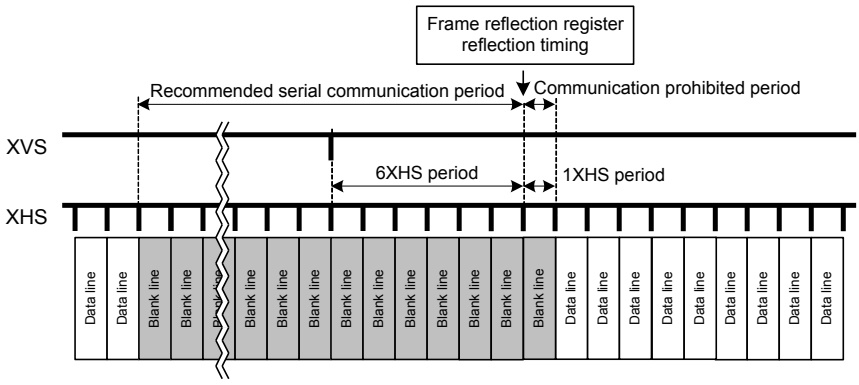
Chip ID	Start address	Data	Data	Data	…
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

Type and Description

Type	Description
Chip ID	02h: Write to the CID = 02h register 03h: Write to the CID = 03h register 04h: Write to the CID = 04h register 82h: Read from the CID = 02h register 83h: Read from the CID = 03h register 84h: Read from the CID = 04h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing (4-wire)

Perform serial communication in sensor standby mode or within in the 6XHS period after the falling edge of XVS from the blanking line output start time after valid line of one frame is finished. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.)



Register Write and Read (4-wire)

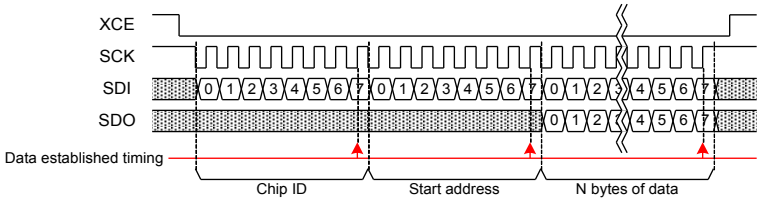
Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input the Chip ID (CID = 02h or 03h or 04h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
(7) Set XCE High to end communication.

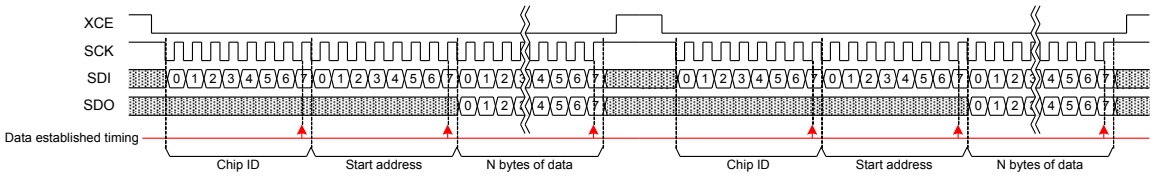
Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.
(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
(3) Input Chip ID (CID = 82h or 83h or 84h) to the first byte. If the Chip ID differs, subsequent data is ignored.
(4) Input the start address to the second byte. The address is automatically incremented.
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
(7) Set XCE High to end communication.

Note) When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times.



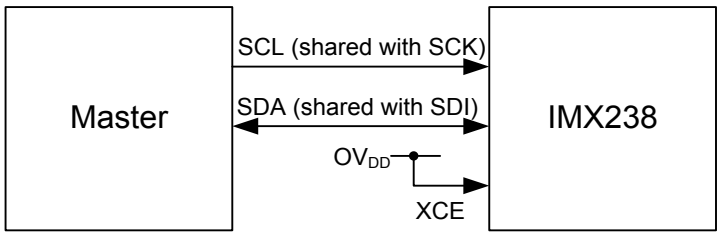
Serial Communication (Continuous Addresses)



Serial Communication (Discontinuous Addresses)

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

SLAVE Address

MSB							LSB
0	0	1	1	0	1	0	R/W

* R/W is data direction bit

R/W

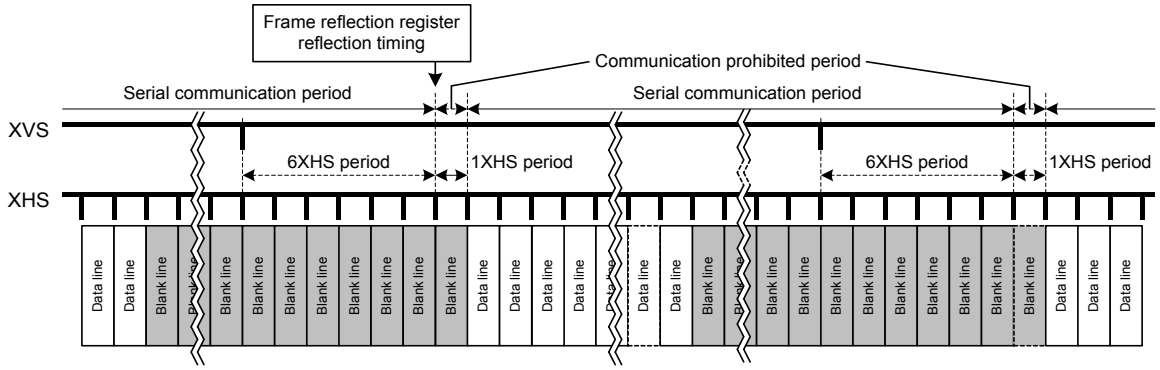
R/W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SCL (common to SCK)	C5	Serial clock input
SDA (common to SDI)	D7	Serial data communication

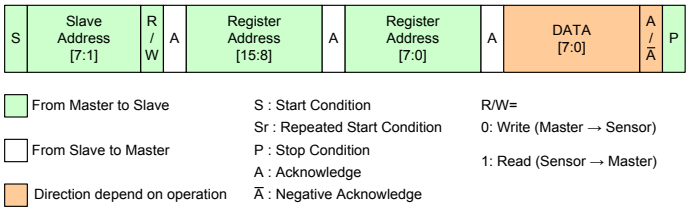
Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed excluding during the period when communication is prohibited from the falling edge of XVS to 6H after (1H period). For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REG_HOLD function is recommended for register setting using I^2C communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”.



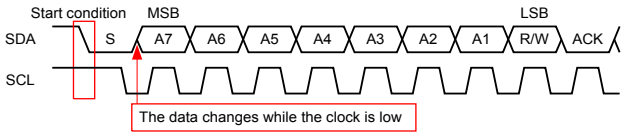
I²C Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

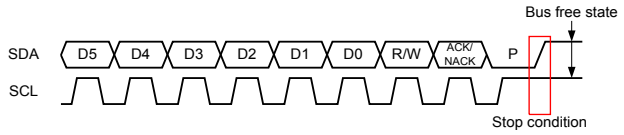


Communication protocol

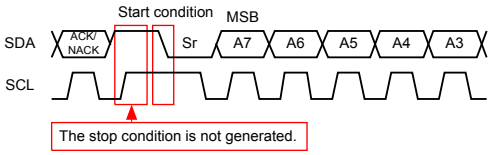
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start Condition is defined by SDA changing from High to Low while SCL is High. When the Stop Condition is not generated in the previous communication phase and Start Condition for the next communication is generated, that Start Condition is recognized as a Repeated Start Condition.



Start Condition

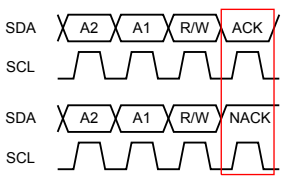


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



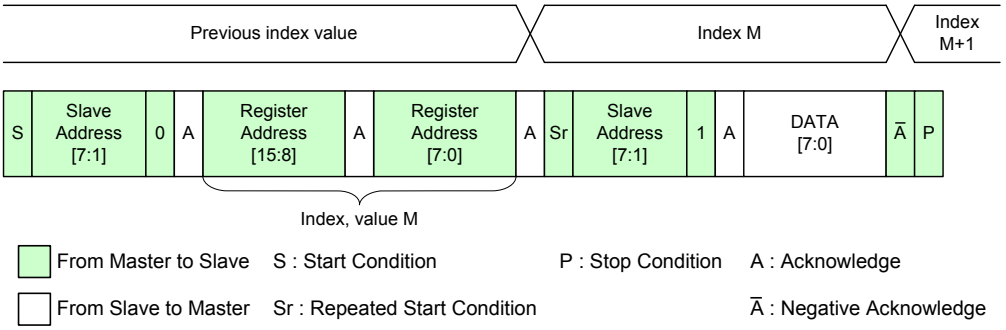
Acknowledge and Negative Acknowledge

I²C Serial Communication Read / Write Operation

This sensor supports the following four read operations and two write operations.

Single Read from Random Location

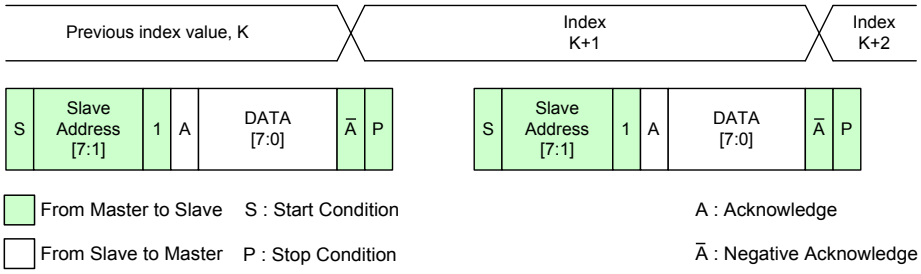
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the Start Condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication.



Single Read from Random Location

Single Read from Current Location

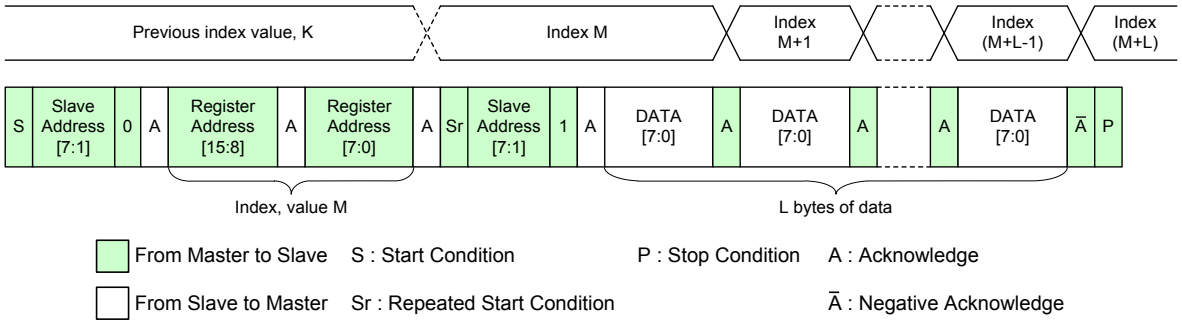
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read / write is performed, the index is incremented by the subsequent Acknowledge / Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

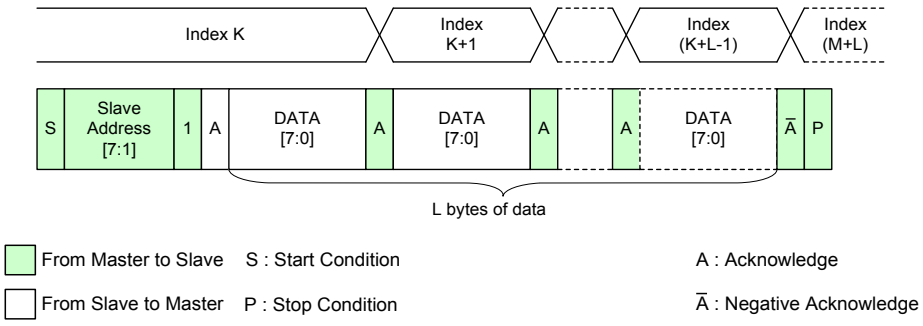
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

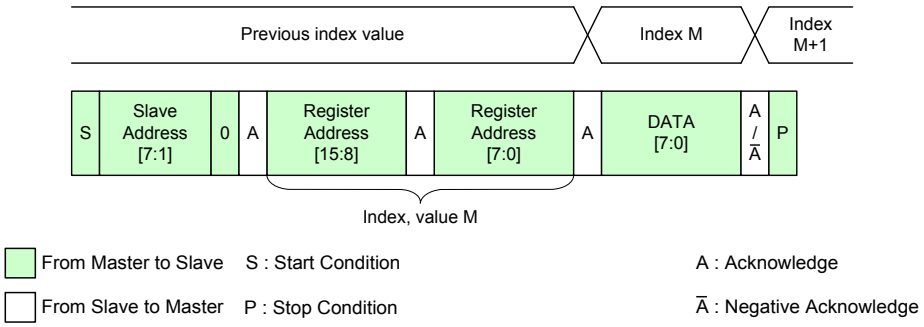
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

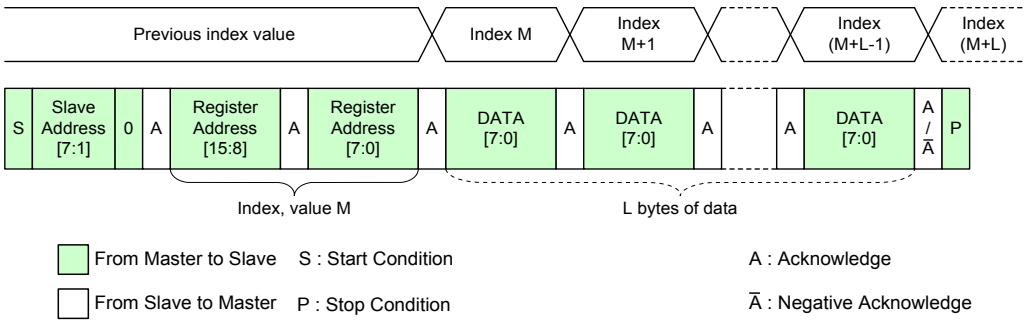
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

In 4-wire serial communication, this sensor has a total of 765 bytes of registers, composed of registers with addresses 00h to FFh that correspond to Chip ID = 02h (write mode) / 82h (read mode), registers with addresses 00h to FFh that correspond to Chip ID = 03h (write mode) / 83h (read mode), and registers with addresses 00h to FFh that correspond to Chip ID = 04h (write mode) / 84h (read mode). Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 765 bytes. I^2C communication has also the same number of registers, so perform the same way above. See the table below and on the following pages for 4-wire serial communication and I^2C communication address correspondence.

(1) 4-wire serial communication: Chip ID = 02h / I^2C communication: 30**h

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h	3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
01h	3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
02h	3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
03h	3003h	0	SW_RESET	Software reset 0: Operating 1: Reset	0h	00h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
04h	3004h	[7:0]		Fixed to "10h"	10h	10h	
05h	3005h	[7:0]		Set to "01h"	00h	00h	
06h	3006h	[7:0]		Fixed to "00h"	00h	00h	

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
07h	3007h	0	VREVERSE	Vertical (V) direction readout inversion control 0: Normal, 1: Inverted	0h	00h	V
		1	HREVERSE	Horizontal (H) direction readout inversion control 0: Normal, 1: Inverted	0h		V
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	WINMODE [1:0]	Window mode setting 0: All-pix scan mode 1: 720p mode 2: Window cropping mode (from all-pix scan mode) 3: Window cropping mode (from 720p mode)	0h		V
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
08h	3008h	[7:0]		Fixed to "10h"	10h	10h	
09h	3009h	0	FRSEL [1:0]	Frame rate (data rate) setting 1: 60 fps mode, 2: 30 fps mode 0, 3: Setting prohibited	2h	02h	V
		1					
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
0Ah	300Ah	0	BLKLEVEL [8:0]	LSB	03Ch	3Ch	V
		1					
		2					
		3					
		4		Black level offset value setting			
		5					
		6					
		7					
0Bh	300Bh	0		MSB		00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
0Ch	300Ch	[7:0]		Fixed to "00h"	00h	00h	
0Dh	300Dh	[7:0]		Fixed to "20h"	20h	20h	
0Eh	300Eh	[7:0]		Fixed to "01h"	01h	01h	
0Fh	300Fh	[7:0]		Fixed to "01h"	01h	01h	
10h	3010h	[7:0]		Fixed to "39h"	39h	39h	
11h	3011h	0	LP_MODE [7:0]	LSB	00h	00h	V
		1					
		2					
		3		Light performance mode setting 00h: High light performance mode 14h: Low light performance mode (recommend)			
		4					
		5					
		6					
		7		MSB			
12h	3012h	[7:0]		Fixed to "50h"	50h	50h	
13h	3013h	[7:0]		Fixed to "00h"	00h	00h	
14h	3014h	0	GAIN [7:0]	LSB	00h	00h	V
		1					
		2					
		3		Gain setting (- 6.0 dB – 42.0 dB / 0.3 dB step)			
		4					
		5					
		6					
		7		MSB			

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
15h	3015h	[7:0]		Fixed to "00h"	00h	00h	
16h	3016h	[7:0]		Fixed to "08h"	08h	08h	
17h	3017h	[7:0]		Set to "01h"	00h	00h	
18h	3018h	0	VMAX [15:0]	LSB Vertical span setting (Effective in master mode. Invalid in slave mode) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions"	0444h	44h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
19h	3019h	0				04h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
08h	3008h	[7:0]		Fixed to "00h"	00h	00h	
1Bh	301Bh	0	HMAX [15:0]	LSB Horizontal span setting (Effective in master mode. Invalid in slave mode) For details, see the item of "Slave Mode and Master Mode" in the section of "Description of Various Functions".	0CE4h	E4h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
1Ch	301Ch	0				0Ch	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
1Dh	301Dh	[7:0]		Set to "FFh"	14h	14h	
1Eh	301Eh	[7:0]		Set to "01h"	02h	02h	
1Fh	301Fh	[7:0]		Fixed to "00h"	00h	00h	
20h	3020h	0	SHS1 [15:0]	LSB Storage time adjustment Designated in line units	0000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
21h	3021h	0				00h	
		1					
		2					
		3					
		4					
		5					
		6					
		7		MSB			
22h to 35h	3022h to 3035h	[7:0] to [7:0]		Do not rewrite			

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
36h	3036h	0	WINWV_OB[4:0]	LSB In window cropping mode VOPB size designation (Vertical direction) MSB	14h	14h	V
		1					
		2					
		3					
		4					
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
37h	3037h	[7:0]		Fixed to "00h"	00h	00h	
38h	3038h	0	WINPV [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
39h	3039h	0				00h	
		1					
		2		MSB			
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
3Ah	303Ah	0	WINWV [10:0]	LSB In window cropping mode Cropping size designation (Vertical direction)	419h	19h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Bh	303Bh	0				04h	
		1					
		2		MSB			
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
3Ch	303Ch	0	WINPH [10:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (horizontal position) Set to become the multiple of four	000h	00h	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Dh	303Dh	0		MSB		00h	
		1					
		2					
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
3Eh	303Eh	0	WINWH [10:0]	LSB In window cropping mode Cropping size designation (horizontal direction) Set to become the multiple of eight and plus four	51Ch	1Ch	V
		1					
		2					
		3					
		4					
		5					
		6					
		7					
3Fh	303Fh	0		MSB		05h	
		1					
		2					
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		

40h	3040h	[7:0]		Fixed to "00h"	00h	00h	
41h	3041h	[7:0]		Fixed to "00h"	00h	00h	
42h	3042h	[7:0]		Fixed to "00h"	00h	00h	
43h	3043h	[7:0]		Fixed to "00h"	00h	00h	
44h	3044h	0		Set to “1”	0h	00h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	OPORTSEL [3:0]	Output system selection 0h: Parallel CMOS SDR output 6h: Parallel low-voltage LVDS DDR output Ch: Serial low-voltage LVDS 1 ch DDR output Dh: Serial low-voltage LVDS 2 ch DDR output Eh: Serial low-voltage LVDS 4 ch DDR output Others: Setting prohibited	0h		Immediately
		5					
		6					
		7					

45h	3045h	[7:0]		Fixed to "01h"	01h	01h	

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
46h	3046h	0		Fixed to "0"	0h	00h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	XVSLNG [1:0]	XVS pulse width setting in master mode (Invalid in slave mode) 0: 1H, 1: 2H, 2: 4H, 3: 8H	0h		Immediately
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
47h	3047h	0		Fixed to "0"	0h	08h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "1"	1h		
		4	XHSLNG [1:0]	XHS pulse width setting in master mode (Invalid in slave mode) 0: Min. to 3: Max.	0h		Immediately
		5					
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
48h	3048h	[7:0]		Fixed to "00h"	00h	00h	
49h	3049h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Output High setting 2: VSYNC output Others: Setting prohibited	0h	00h	Immediately
		1					
		2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Output High setting 2: HSYNC output Others: Setting prohibited	0h		Immediately
		3					
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
4Ah to 53h	304Ah to 3053h	[7:0] to [7:0]		Do not rewrite			
54h	3054h	[7:0]		Set to "63h"	61h	61h	
55h to 5Ah	3055h to 305Ah	[7:0] to [7:0]		Do not rewrite			

Address		Bit	Register Name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
5Bh	305Bh	0	INCKSEL1	INCK setting 1 0: 37.125 MHz or 74.25 MHz 1: 27 MHz or 54 MHz	1h	01h	Immediately
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4		Fixed to "0"	0h		
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
5Ch	305Ch	[7:0]		Fixed to "20h"	20h	20h	
5Dh	305Dh	0		Fixed to "0"	0h	10h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	INCKSEL2	INCK setting 2 0: Input 27 MHz or 37.125 MHz 1: Input 54 MHz or 74.25 MHz	1h		Immediately
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
5Eh	305Eh	[7:0]		Fixed to "2Ch"	2Ch	2Ch	
5Fh	305Fh	0		Fixed to "0"	0h	10h	
		1		Fixed to "0"	0h		
		2		Fixed to "0"	0h		
		3		Fixed to "0"	0h		
		4	INCKSEL3	INCK setting 3 0: 27 [MHz] 1: 54 [MHz] When INCK frequency is 37.125 MHz or 74.25 MHz, this register is invalid.	1h		Immediately
		5		Fixed to "0"	0h		
		6		Fixed to "0"	0h		
		7		Fixed to "0"	0h		
60h	3060h	[7:0]		Fixed to "00h"	00h	00h	
61h	3061h	[7:0]		Fixed to "21h"	21h	21h	
62h	3062h	[7:0]		Fixed to "08h"	08h	08h	
63h to BEh	3063h to 30BEh	[7:0] to [7:0]		Do not rewrite			
BFh	30BFh	[7:0]		Set to "1Fh"	10h	10h	
C0h to FFh	30C0h to 30FFh	[7:0] to [7:0]		Do not rewrite			

*1 There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.

*2 Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h and 04h. (In I^2C communication, the address 3000h to 30FFh, 3100h to 31FFh and 3200h to 32FFh should be available.)

(2) 4-wire serial communication: Chip ID = 03h / I²C communication: 31**h

Address		Setting value	Default value after reset
4-wire	I²C		
12h	3112h	00h	02h
1Dh	311Dh	07h	08h
23h	3123h	07h	0Fh
26h	3126h	DFh	5Fh
47h	3147h	87h	B4h
C5h to D4h	31C5h to 31D4h	Communication prohibited*2	

*1 Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h and 04h. (In I²C communication, the address 3000h to 30FFh, 3100h to 31FFh and 3200h to 32FFh should be available.)

*2 These registers are communication prohibited. Do not write and read.

(3) 4-wire serial communication: Chip ID = 04h / I²C communication: 32**h

Address		Setting value	Default value after reset
4-wire	I²C		
03h	3203h	CDh	B4h
07h	3207h	4Bh	32h
09h	3209h	E9h	ECh
13h	3213h	1Bh	E5h
15h	3215h	EDh	FFh
16h	3216h	01h	0Fh
18h	3218h	09h	0Fh
1Ah	321Ah	19h	E3h
1Bh	321Bh	A1h	41h
1Ch	321Ch	11h	1Eh
27h	3227h	00h	40h
28h	3228h	05h	03h
29h	3229h	ECh	D3h
2Ah	322Ah	40h	B0h
2Bh	322Bh	11h	0Fh
2Dh	322Dh	22h	06h
2Eh	322Eh	00h	40h
2Fh	322Fh	05h	03h
31h	3231h	ECh	D3h
32h	3232h	40h	B0h
33h	3233h	11h	0Fh
35h	3235h	23h	07h
36h	3236h	B0h	F0h
37h	3237h	04h	02h
39h	3239h	24h	08h
3Ah	323Ah	30h	70h
3Bh	323Bh	04h	02h
3Ch	323Ch	EDh	D4h
3Dh	323Dh	C0h	30h
3Eh	323Eh	10h	0Fh
40h	3240h	44h	28h
41h	3241h	A0h	E0h
42h	3242h	04h	02h
43h	3243h	0Dh	F4h
44h	3244h	31h	A0h
45h	3245h	11h	0Fh
47h	3247h	ECh	D3h
48h	3248h	D0h	40h
49h	3249h	1Dh	1Ch
52h	3252h	FFh	D4h
53h	3253h	FFh	20h
54h	3254h	FFh	1Dh
55h	3255h	02h	00h
56h	3256h	54h	35h
57h	3257h	60h	D0h
58h	3258h	1Fh	1Dh
5Ah	325Ah	A9h	90h
5Bh	325Bh	50h	C0h
5Ch	325Ch	0Ah	08h

Address		Setting value	Default value after reset
4-wire	I²C		
5Dh	325Dh	25h	0Ch
5Eh	325Eh	11h	81h
5Fh	325Fh	12h	10h
61h	3261h	9Bh	6Eh
66h	3266h	D0h	C0h
67h	3267h	08h	07h
6Ah	326Ah	20h	30h
6Bh	326Bh	0Ah	08h
6Eh	326Eh	20h	30h
6Fh	326Fh	0Ah	08h
72h	3272h	20h	30h
73h	3273h	0Ah	08h
75h	3275h	ECh	D3h
7Dh	327Dh	A5h	8Ch
7Eh	327Eh	20h	90h
7Fh	327Fh	0Ah	08h
81h	3281h	EFh	D6h
82h	3282h	C0h	30h
83h	3283h	0Eh	0Dh
85h	3285h	F6h	DDh
8Ah	328Ah	60h	D0h
8Bh	328Bh	1Fh	1Dh
8Dh	328Dh	BBh	A2h
8Eh	328Eh	90h	00h
8Fh	328Fh	0Dh	0Ch
90h	3290h	39h	20h
91h	3291h	C1h	31h
92h	3292h	1Dh	1Ch
94h	3294h	C9h	B0h
95h	3295h	70h	E0h
96h	3296h	0Eh	0Ch
97h	3297h	47h	2Eh
98h	3298h	A1h	11h
99h	3299h	1Eh	1Dh
9Bh	329Bh	C5h	ACh
9Ch	329Ch	B0h	20h
9Dh	329Dh	0Eh	0Dh
9Eh	329Eh	43h	2Ah
9Fh	329Fh	E1h	51h
A0h	32A0h	1Eh	1Dh
A2h	32A2h	BBh	9Ch
A3h	32A3h	10h	20h
A4h	32A4h	0Ch	0Ah
A6h	32A6h	B3h	94h
A7h	32A7h	30h	40h
A8h	32A8h	0Ah	08h
A9h	32A9h	29h	10h
AAh	32AAh	91h	01h
ABh	32ABh	11h	10h

Address		Setting value	Default value after reset
4-wire	I²C		
ADh	32ADh	B4h	95h
AEh	32AEh	40h	50h
AFh	32AFh	0Ah	08h
B0h	32B0h	2Ah	11h
B1h	32B1h	A1h	11h
B2h	32B2h	11h	10h
B4h	32B4h	ABh	8Ch
B5h	32B5h	B0h	C0h
B6h	32B6h	0Bh	09h
B7h	32B7h	21h	08h
B8h	32B8h	11h	81h
B9h	32B9h	13h	11h
BBh	32BBh	ACh	8Dh
BCh	32BCh	C0h	D0h
BDh	32BDh	0Bh	09h
BEh	32BEh	22h	09h
BFh	32BFh	21h	91h
C0h	32C0h	13h	11h
C2h	32C2h	ADh	8Eh
C3h	32C3h	10h	20h
C4h	32C4h	0Bh	09h
C5h	32C5h	23h	0Ah
C6h	32C6h	71h	E1h
C7h	32C7h	12h	10h
C9h	32C9h	B5h	96h
CAh	32CAh	90h	A0h
CBh	32CBh	0Bh	09h
CCh	32CCh	2Bh	12h
CDh	32CDh	F1h	61h
CEh	32CEh	12h	11h
D0h	32D0h	BBh	9Ch
D1h	32D1h	10h	20h
D2h	32D2h	0Ch	0Ah
D4h	32D4h	E7h	CEh
D5h	32D5h	90h	00h
D6h	32D6h	0Eh	0Dh
D8h	32D8h	45h	2Ch
D9h	32D9h	11h	81h
DAh	32DAh	1Fh	1Dh
EBh	32EBh	A4h	84h
ECh	32ECh	60h	D0h
EDh	32EDh	1Fh	1Dh

* Do not rewrite to addresses not listed in the Register Map. Doing so may result in operation errors. However, in 4-wire serial communication, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for CID = 02h, 03h and 04h. (In I²C communication, the address 3000h to 30FFh, 3100h to 31FFh and 3200h to 32FFh should be available.)

Readout Drive Modes

The table below lists the operating modes available with this sensor.

List of Operation Modes and Output Rates for Parallel Output

Operating mode	INCK [MHz]	Frame rate [fps]	Data rate [Mpix/s]	Output mode : Parallel		AD conversion (bit)	Output bit width (bit)	Number of recording pixels		Total number of pixels		Number of output vertical lines and horizontal pixels		Number of INCK in 1H	
				CMOS	Low-voltage LVDS			Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	27 MHz or 37.125 MHz	54 MHz or 74.25 MHz
All-pixel scan mode	37.125 / 74.25	30.00	74.25	○	○	12	12	1280	1024	1312	1069	2250	1100	1125	2250
		60.00	148.50	N/A	○	12	12							562.5	1125
	27 / 54	29.97	54.00	○	○	12	12	1280	1024	1312	1069	1650	1092	825	1650
		59.94	108.00	N/A	○	12	12							412.5	825
		25.00	54.00	○	○	12	12	1280	1024	1312	1069	1800	1200	900	1800
		50.00	108.00	N/A	○	12	12							450	900
720p-HD mode	37.125 / 74.25	30.00	37.125	○	○	12	12	1280	720	1312	741	1650	750	1650	3300
		60.00	74.25	○	○	12	12							825	1650

* N/A: Mode not supported

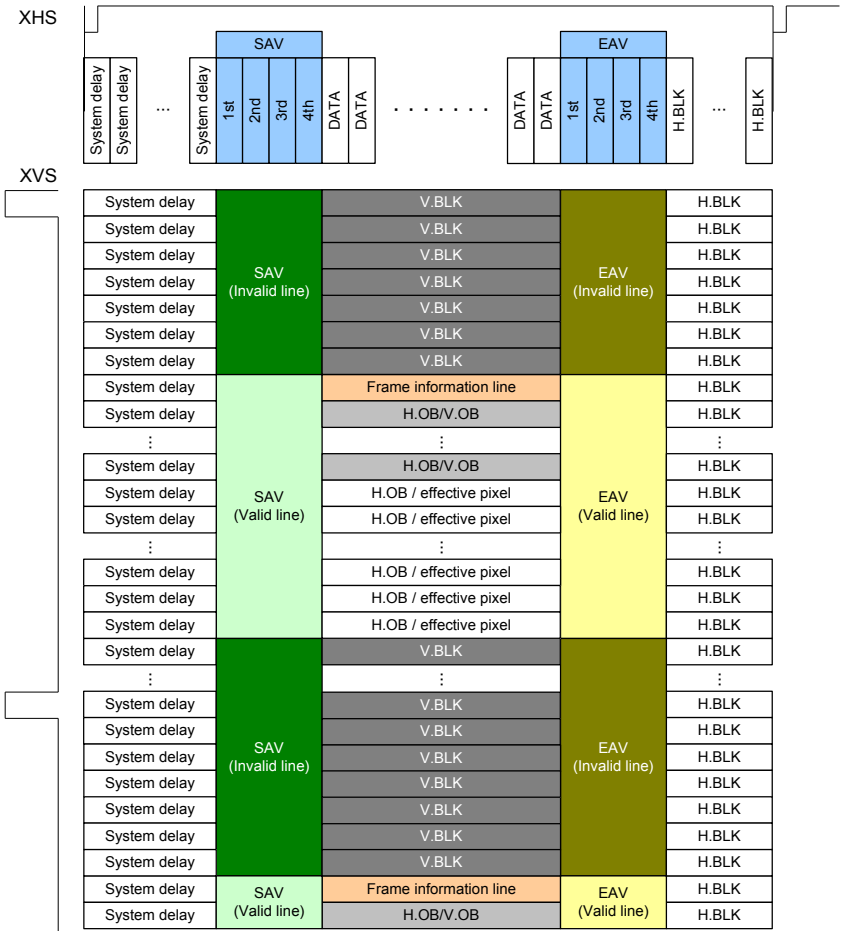
List of Operation Modes and Output Rates for Serial Output

Operating mode	INCK [MHz]	Frame rate [fps]	Data rate [Mpix/s]	Output mode: Serial			AD conversion (bit)	Output bit width (bit)	Number of recording pixels		Total number of pixels		Number of output vertical lines and horizontal pixels		Number of INCK in 1H	
				Low-voltage LVDS 1 ch	Low-voltage LVDS 2 ch	Low-voltage LVDS 4 ch			Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	27 MHz or 37.125 MHz	54 MHz or 74.25 MHz
All-pixel scan mode	37.125 / 74.25	30.00	594.00	○	N/A	N/A	12	12	1280	1024	1312	1069	1500	1100	1125	2250
			297.00	N/A	○	N/A	12	12								
			148.50	N/A	N/A	○	12	12								
		60.00	594.00	N/A	○	N/A	12	12							562.5	1125
			297.00	N/A	N/A	○	12	12								
	27 / 54	29.97	432.00	N/A	○	N/A	12	12	1280	1024	1312	1069	2200	1092	825	1650
			216.00	N/A	N/A	○	12	12								
		59.94	432.00	N/A	N/A	○	12	12							412.5	825
		25.00	432.00	N/A	○	N/A	12	12	1280	1024	1312	1069	2400	1200	900	1800
			216.00	N/A	N/A	○	12	12								
		50.00	432.00	N/A	N/A	○	12	12							450	900
720p-HD mode	37.125 / 74.25	30.00	594.00	○	N/A	N/A	12	12	1280	720	1312	741	2200	750	1650	3300
			297.00	N/A	○	N/A	12	12								
			148.50	N/A	N/A	○	12	12								
		60.00	594.00	N/A	○	N/A	12	12							825	1650
			297.00	N/A	N/A	○	12	12								

* N/A: Mode not supported

Sync Code

The sync code is added just before and after “dummy signal + OB signal + effective pixel data”. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd.
(BLK: Blanking period)



Sync Code Output Timing

List of Sync Code

Sync code	1st code	2nd code	3rd code	4th code
	12 bit	12 bit	12 bit	12 bit
SAV (Valid line)	FFFh	000h	000h	800h
EAV (Valid line)	FFFh	000h	000h	9D0h
SAV (Invalid line)	FFFh	000h	000h	AB0h
EAV (Invalid line)	FFFh	000h	000h	B60h

(Note 1) 12 bit is the value output to the DOP/M [11:0] when parallel output.
(The DOM [11:0] outputs Low in CMOS parallel output.)
(Note 2) They are output to each channel seriously in MSB first when low-voltage LVDS serial.
For details, see the item of "Signal output" and "Output pin setting".

Sync Code Output Timing

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.

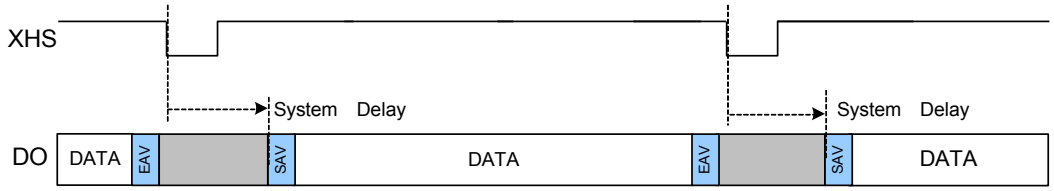


Image Data Output Format

All-pixel Scan Mode

All the pixel signals of sensor are read.

Register List of All-pixel Mode Setting

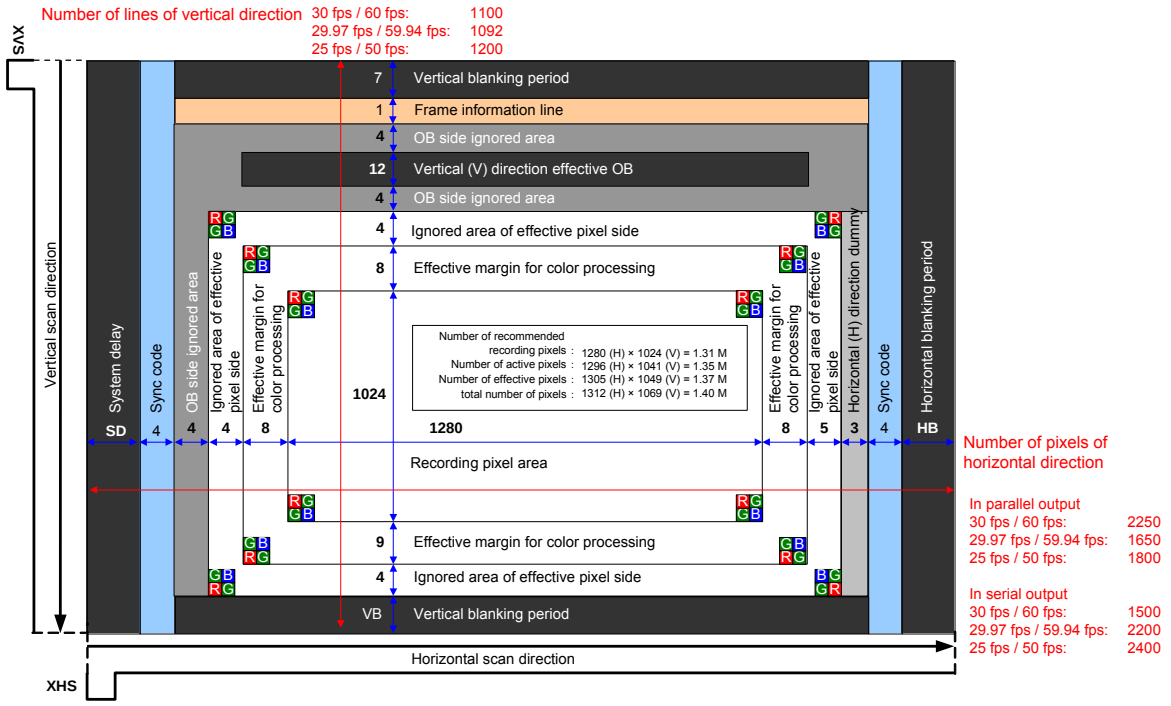
Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
WINMODE [1:0]	—	07h	[5:4]	0h	0h	1.3 M mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below and the next page.	60 fps mode or 30 fps mode
VMAX [15:0]	VMAX [7:0]	18h	[7:0]	0444h (1092d)	See below and the next page.	Vertical (V) direction line number designation (Effective in master mode. Invalid in slave mode)
	VMAX [15:8]	19h	[7:0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0CE4h (3300d)	See below and the next page.	Horizontal (H) direction pixel number designation (Effective in master mode. Invalid in slave mode)
	HMAX [15:8]	1Ch	[7:0]			
OPORTSEL [3:0]	-	44h	[7:4]	0h	See below and the next page.	Parallel CMOS / Parallel low-voltage LVDS / Serial low-voltage LVDS selection
INCKSEL1	-	5Bh	[0]	1h	See below and the next page.	INCK setting
INCKSEL2	-	5Dh	[4]	1h	0h	Input frequency is 27 [MHz] or 37.125 [MHz].
					1h	Input frequency is 54 [MHz] or 74.25 [MHz].
INCKSEL3	—	5Fh	[4]	1h	0h	Input frequency is 27 [MHz]
					1h	Input frequency is 54 [MHz]

Detailed Register List of All-pixel Mode Setting for Parallel Output

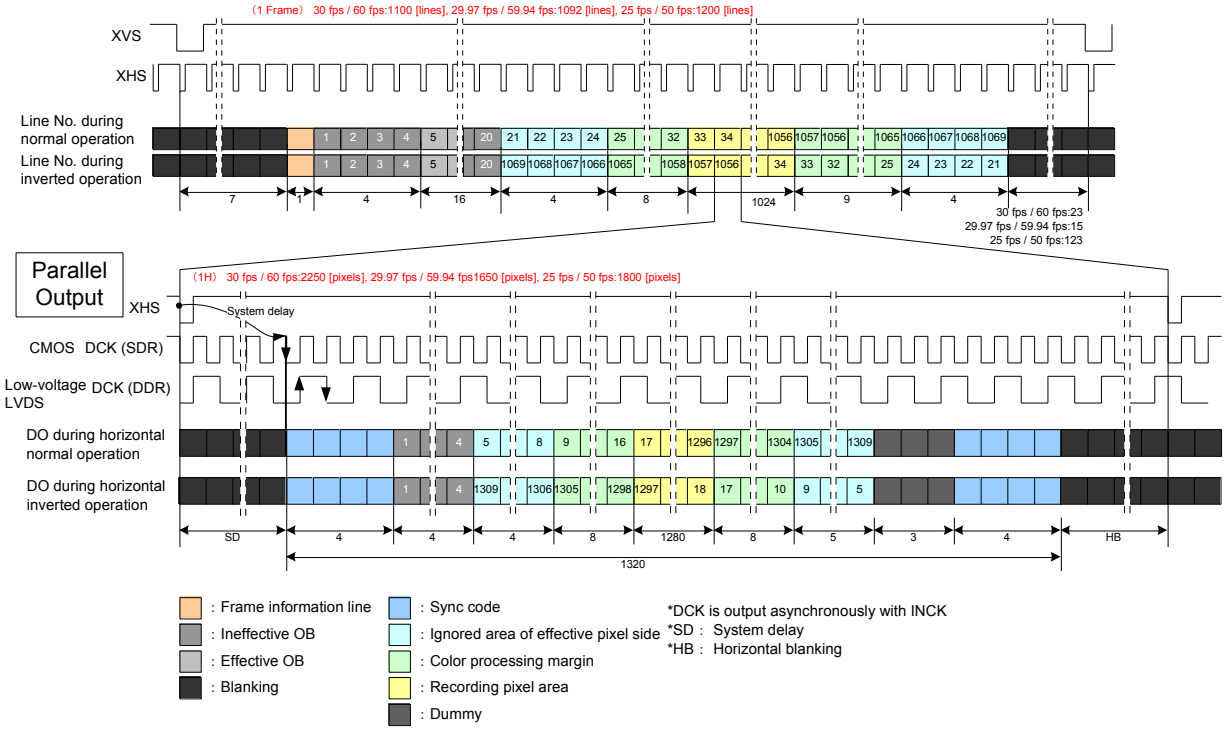
INCK [MHz]	Output format	Output frame rate (fps)	Output data bit Width	FRSEL [1:0]	VMAX [15:0]		HMAX [15:0]		OPORTSEL [3:0]	INCKSEL1
					HEX	DEC	HEX	DEC		
37.125 / 74.25	CMOS	30.00	12 bit	2h	044Ch	1100d	1194h	4500d	0h	0h
	Low-voltage LVDS	30.00	12 bit	2h					6h	
		60.00	12 bit	1h			08CAh	2250d		
27 / 54	CMOS	29.97	12 bit	2h	0444h	1092d	0CE4h	3300d	0h	1h
	Low-voltage LVDS	29.97	12 bit	2h					6h	
		59.94	12 bit	1h			0672h	1650d		
	CMOS	25.00	12 bit	2h	04B0h	1200d	0E10h	3600d	0h	
	Low-voltage LVDS	25.00	12 bit	2h					6h	
		50.00	12 bit	1h			0708h	1800d		

Detailed Register List of All-pixel Mode Setting for Serial Output

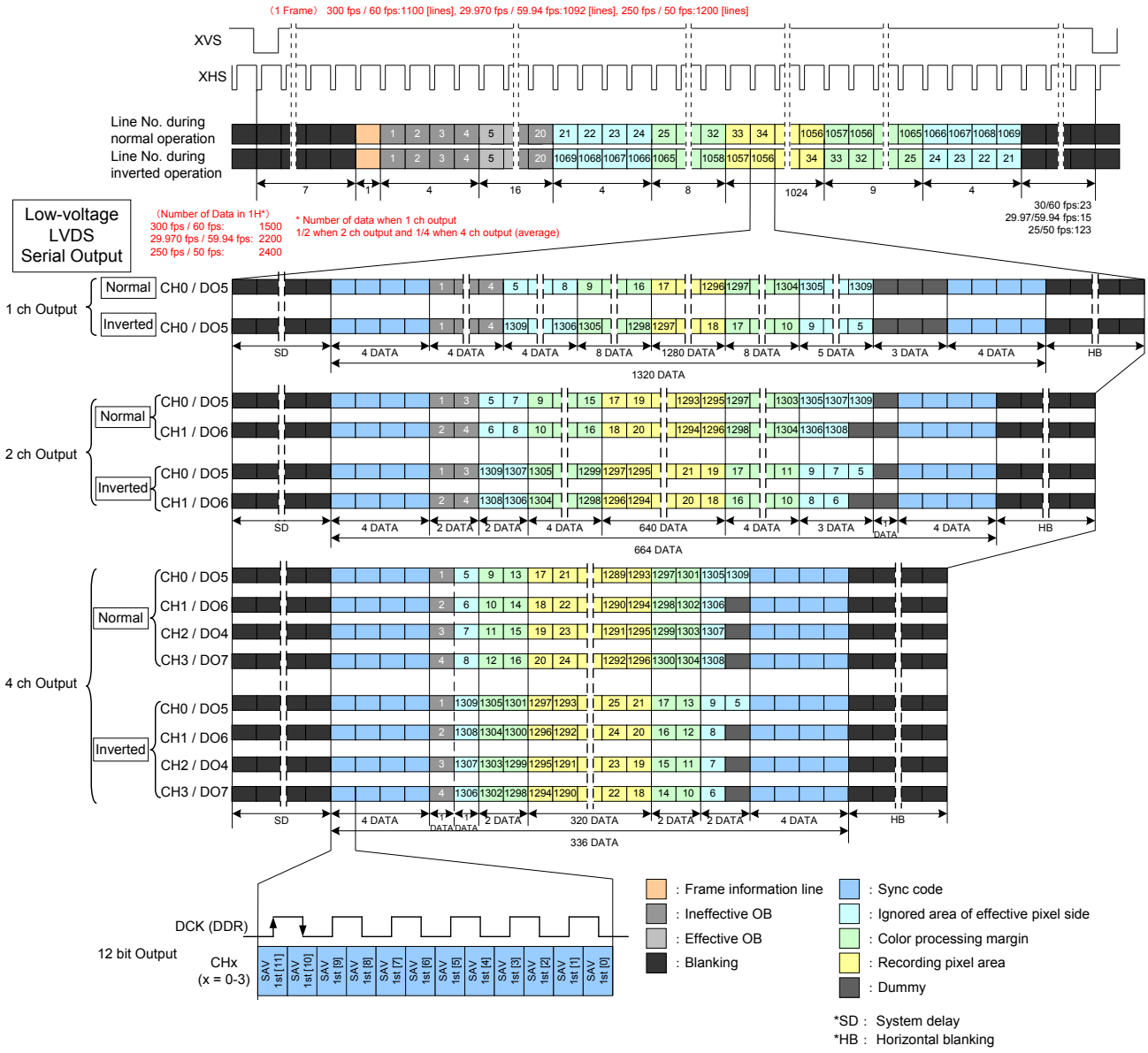
INCK [MHz]	Output format	Output frame rate (fps)	Output data bit Width	FRSEL [1:0]	VMAX [15:0]		HMAX [15:0]		OPORTSEL [3:0]	INCKSEL1
					HEX	DEC	HEX	DEC		
37.125 / 74.25	Low-voltage LVDS serial 1 ch	30.00	12 bit	2h	044Ch	1100d	1194h	4500d	Ch	0h
	Low-voltage LVDS serial 2 ch	30.00	12 bit	2h					Dh	
		60.00	12 bit	1h			08CAh	2250d		
	Low-voltage LVDS serial 4 ch	30.00	12 bit	2h			1194h	4500d	Eh	
		60.00	12 bit	1h			08CAh	2250d		
27 / 54	Low-voltage LVDS serial 2 ch	29.97	12 bit	1h	0444h	1092d	0CE4h	3300d	Dh	1h
	Low-voltage LVDS serial 4 ch	29.97	12 bit	1h					Eh	
		59.94	12 bit	0h			0672h	1650d		
	Low-voltage LVDS serial 2 ch	25.00	12 bit	1h	04B0h	1200d	0E10h	3600d	Dh	
	Low-voltage LVDS serial 4 ch	25.00	12 bit	1h					Eh	
		50.00	12 bit	0h			0708h	1800d		



Pixel Array Image Drawing in All-pixel Scan Mode



Drive Timing Chart for Parallel Output in All-pixel Scan Mode



Drive Timing Chart for Serial Output in All-pixel Scan Mode

720p-HD Mode

The sensor signal is cut out with the angle of view for 720p-HD (1280 × 720) and read

Register List of 720p-HD Mode

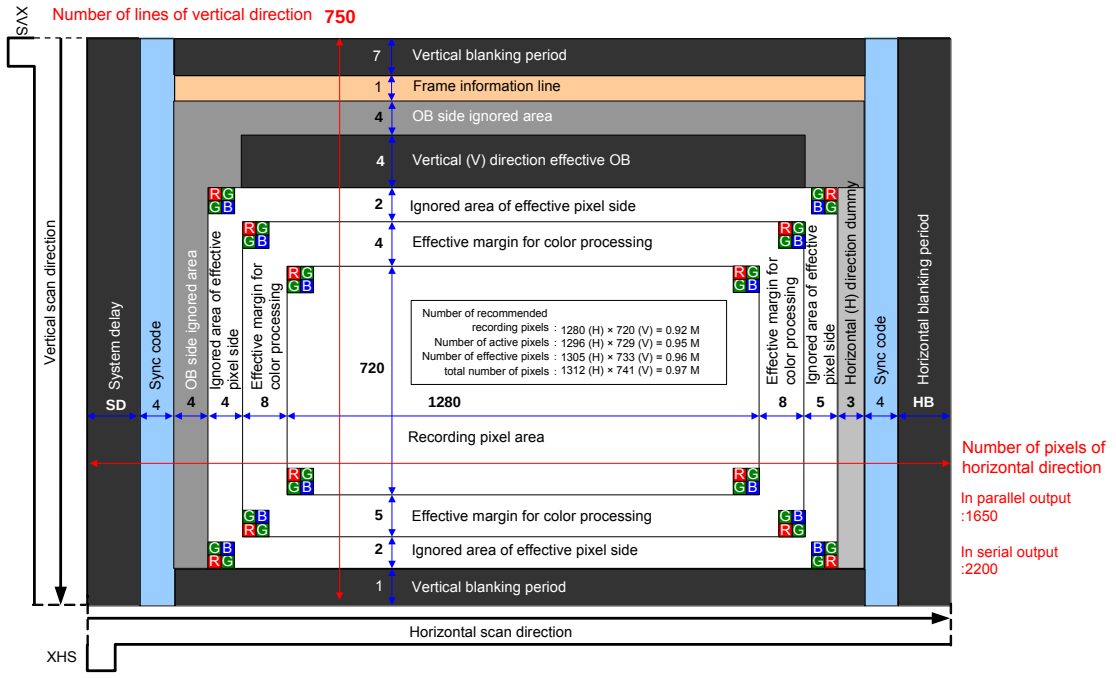
Setting item	Register details			Initial value	Setting value	Function
	Register	Address	bit			
WINMODE [1:0]	—	07h	[5:4]	0h	1h	720p mode
FRSEL [1:0]	—	09h	[1:0]	2h	See below	60 fps mode or 30 fps mode
VMAX [15:0]	VMAX [7:0]	18h	[7:0]	0444h (1092d)	See below	Vertical (V) direction line number designation
	VMAX [15:8]	19h	[7:0]			
HMAX [15:0]	HMAX [7:0]	1Bh	[7:0]	0CE4h (3300d)	See below	Horizontal (H) direction pixel number designation
	HMAX [15:8]	1Ch	[7:0]			
OPORTSEL [3:0]	—	44h	[7:4]	0h	See below	Parallel CMOS / Parallel low-voltage LVDS / Serial low-voltage LVDS selection
INCKSEL1	—	5Bh	[0]	1h	0h	37.125 [MHz] / 74.25 [MHz]
INCKSEL2	—	5Dh	[4]	1h	0h	Input frequency is 37.125 [MHz].
					1h	Input frequency is 74.25 [MHz].

Detailed Register List of 720p-HD Mode Setting for Parallel Output

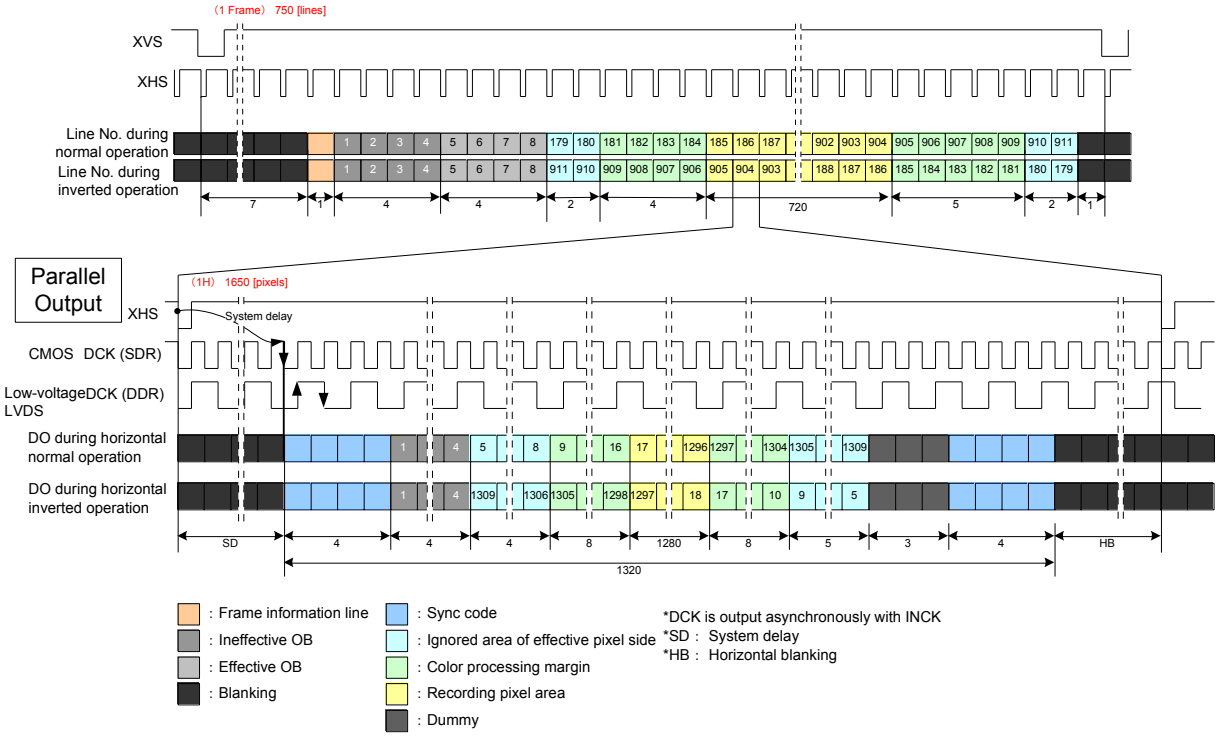
INCK [MHz]	Output format	Output frame rate (fps)	Output data bit Width	FRSEL [1:0]	VMAX [15:0]		HMAX [15:0]		OPORTSEL [3:0]	INCKSEL 1
					HEX	DEC	HEX	DEC		
37.125 / 74.25	CMOS	30.00	12 bit	2h	02EEh	750d	19C8h	6600d	0h	0h
		60.00	12 bit	1h			0CE4h	3300d		
	Low-voltage LVDS	30.00	12 bit	2h			19C8h	6600d	6h	
		60.00	12 bit	1h			0CE4h	3300d		

Detailed Register List of 720p-HD Mode Setting for Serial Output

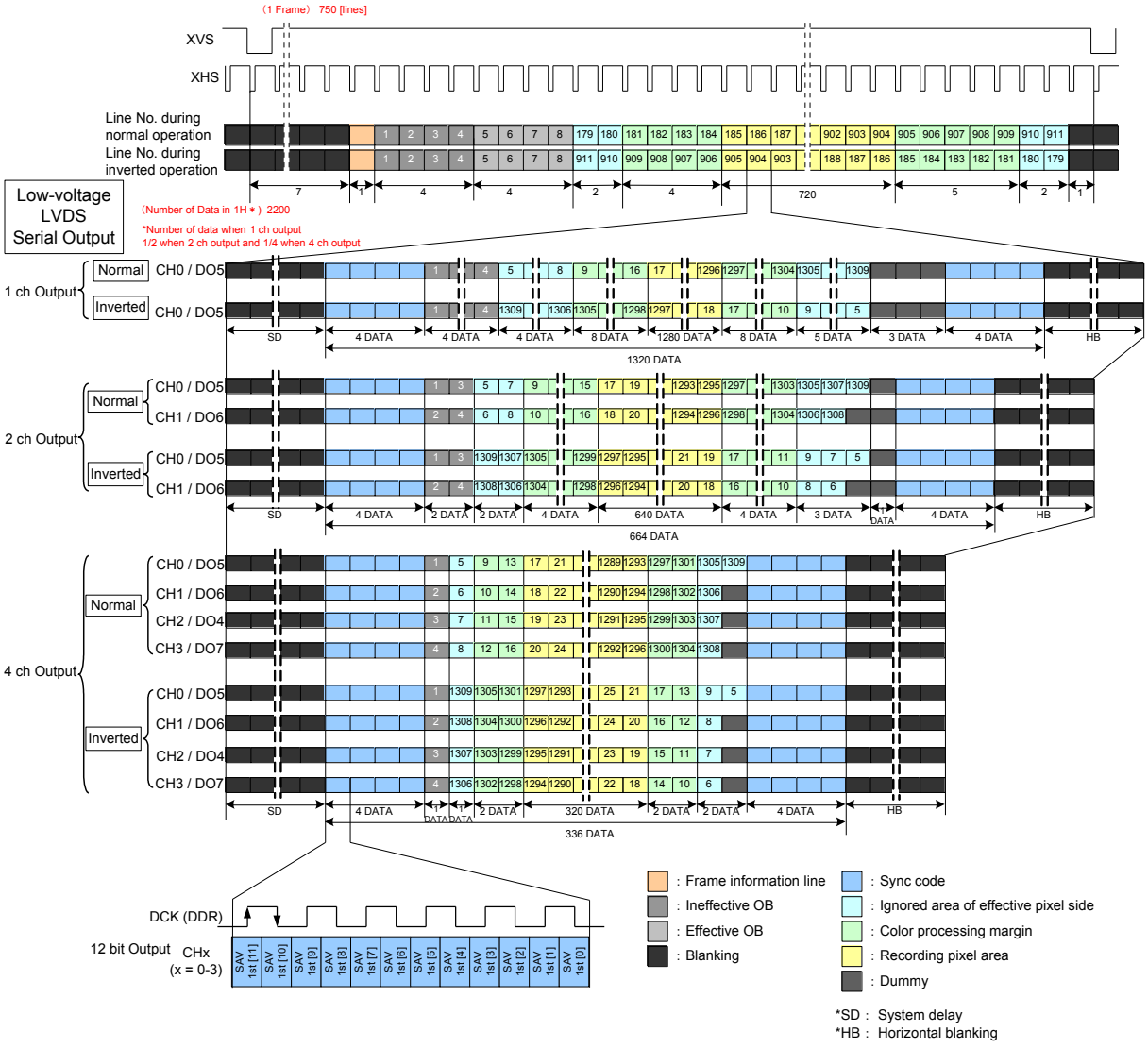
INCK [MHz]	Output format	Output frame rate (fps)	Output data bit Width	FRSEL [1:0]	VMAX [15:0]		HMAX [15:0]		OPORTSEL [3:0]	INCKSEL 1
					HEX	DEC	HEX	DEC		
37.125 / 74.25	Low-voltage LVDS serial 1 ch	30.00	12 bit	2h	02EEh	750d	19C8h	6600d	Ch	0h
	Low-voltage LVDS serial 2 ch	30.00	12 bit	2h					Dh	
		60.00	12 bit	1h			0CE4h	3300d		
	Low-voltage LVDS serial 4 ch	30.00	12 bit	2h			19C8h	6600d	Eh	
		60.00	12 bit	1h			0CE4h	3300d		



Pixel Array Image Drawing in 720p-HD Mode



Drive Timing Chart for Parallel Output in 720p-HD Mode

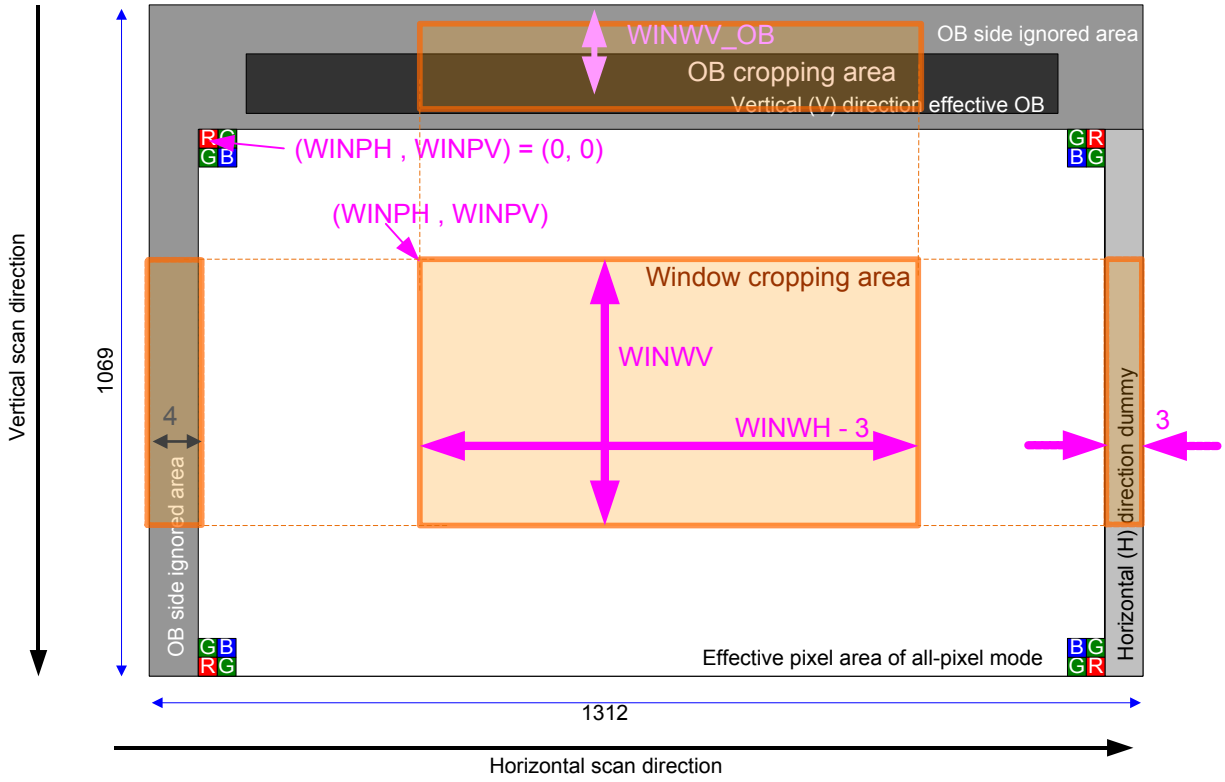


Drive Timing Chart for Serial Output in 720p-HD Mode

Window Cropping Mode

A sensor signals are cropped and read out at arbitrary positions.
Cropping is available at all-pixel scan mode and 720p-HD mode. Horizontal period is fixed to the value for each mode. Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period. In vertical cropping, the number of image data is also output from cropping start line and the frame rate can be adjusted by changing the number of input XVS lines in slave mode or changing register VMAX in master mode.

Window cropping image is shown in the figure below.
Cropping position is set, regarding effective pixel start position as origin (0, 0) in all pixel scan mode.
Only vertical width can be set for OB (horizontal width is the same as the Window cropping width).



Window cropping image from all pixel scan mode

Register List of Window cropping Mode Setting

Setting item	Register details (Chip ID = 02h)			Initial value	Setting value	Function
	Register	Address ( ): I²C	Bit			
WINMODE [1:0]	—	07h (3007h)	[5:4]	0h	2h	Window cropping mode (1.3M mode)
					3h	Window cropping mode (720p mode)
FRSEL [1:0]	—	09h (3009h)	[1:0]	2h	Each mode setting	60 fps or 30 fps mode
VMAX [15:0]	VMAX [7:0]	18h (3018h)	[7:0]	0444h (1092d)	See the next page.	Vertical (V) direction line number designation
	VMAX [15:8]	19h 3019h)	[7:0]			
HMAX [15:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	0CE4h (3300d)	Each mode setting	Horizontal (H) direction pixel number designation
	HMAX [15:8]	1Ch (301Ch)	[7:0]			
WINWV_OB [4:0]	WINWV_OB [4:0]	36h (3036h)	[4:0]	014h (20d)	See the next page.	VOPB Window size designation
WINPV [10:0]	WINPV [7:0]	38h (3038h)	[7:0]	000h	See the next page.	Designation of upper left coordinate for cropping position (Vertical)
	WINPV [10:8]	39h (3039h)	[2:0]			
WINWV [10:0]	WINWV [7:0]	3Ah (303Ah)	[7:0]	419h (1049d)	See the next page.	Cropping size designation (Vertical)
	WINWV [10:8]	3Bh (303Bh)	[2:0]			
WINPH [10:0]	WINPH [7:0]	3Ch (303Ch)	[7:0]	000h	See the next page.	Designation of upper left coordinate for cropping position (Horizontal) (Set to become a multiple of 4)
	WINPH [10:8]	3Dh (303Dh)	[2:0]			
WINWH [10:0]	WINWH [7:0]	3Eh (303Eh)	[7:0]	51Ch (1308d)	See the next page.	Cropping size designation (Horizontal) (Set to become a multiple of 8 and plus 4)
	WINWH [10:8]	3Fh (303Fh)	[2:0]			
OPORTSEL [3:0]	—	44h (3044h)	[7:4]	0h	Each mode setting	Parallel CMOS / Parallel low-voltage LVDS / Serial low-voltage LVDS selection
INCKSEL1	—	5Bh (305Bh)	[0]	1h	Each mode setting	INCK setting
INCKSEL2	—	5Dh (305Dh)	[4]	1h	Each mode setting	INCK setting
INCKSEL3	—	5Fh (305Fh)	[4]	1h	Each mode setting	INCK setting

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

WINPH + WINWH ≤ 1308
380 ≤ WINWH
Set WINPH to a multiple of 4, and set WINWH to a multiple of 8 and plus 4.

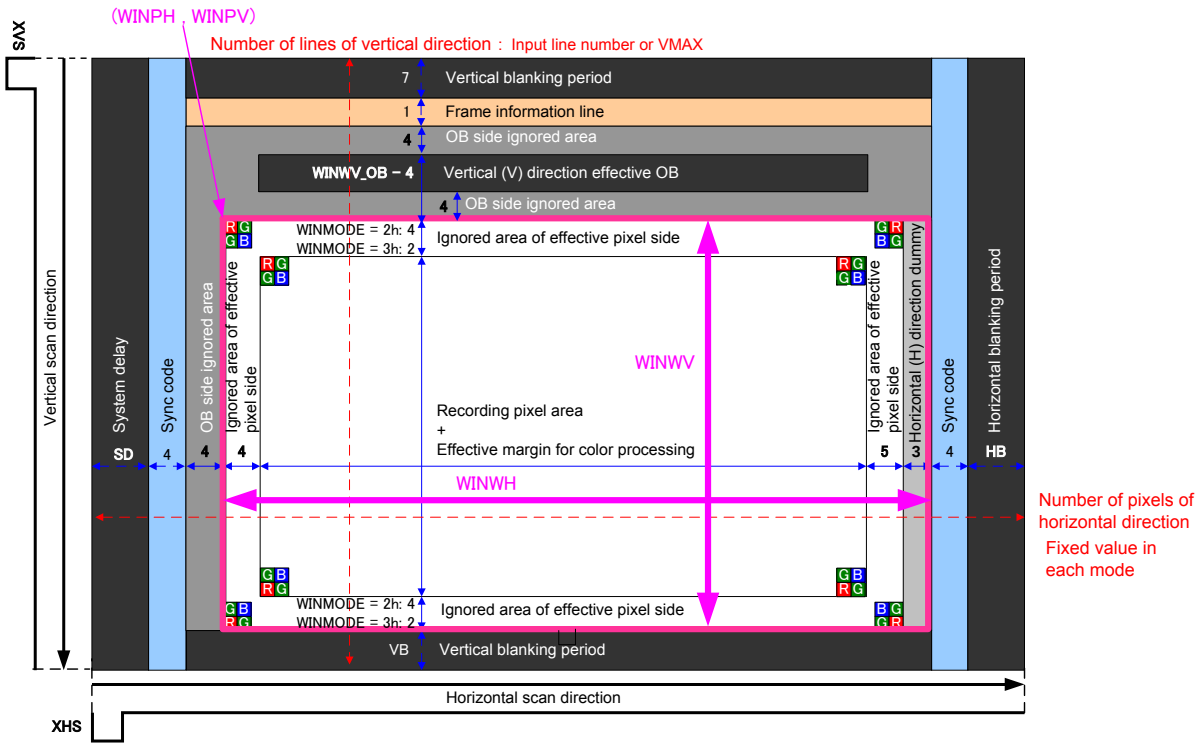
(Number of lines per frame) or VMAX ≥ WINWV_OB + WINWV + 8

However,
8 ≤ WINWV_OB ≤ 20
WINPV + WINWV ≤ 1049
313 ≤ WINWV

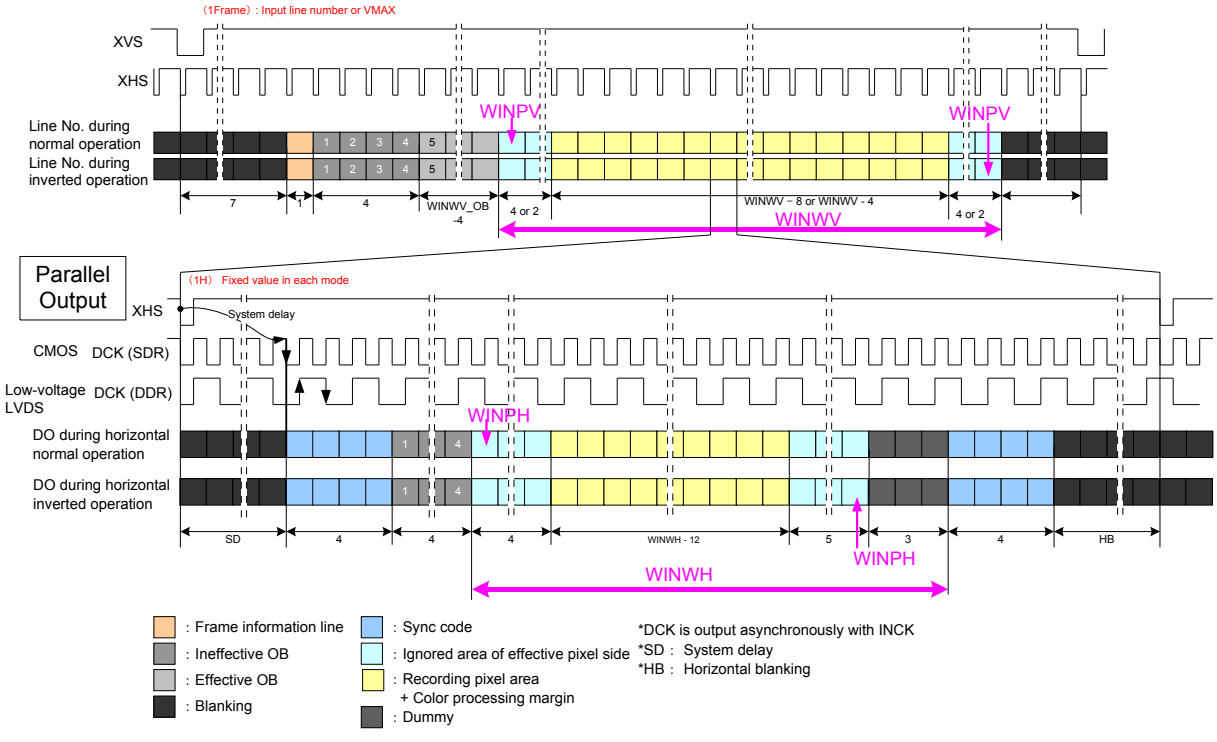
Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (("Number of lines per frame" or VMAX) × (1H period))

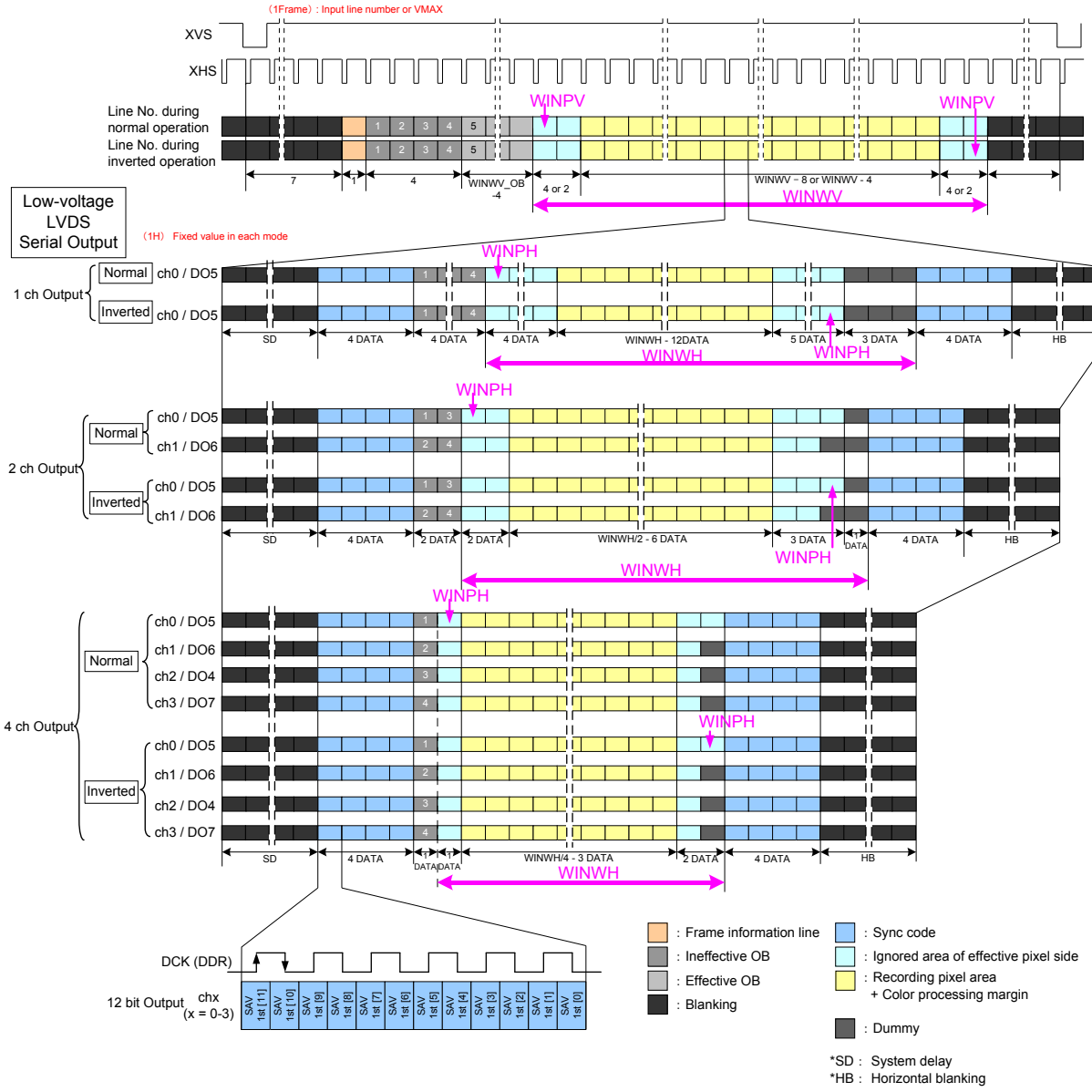
1H period (unit: [µs]): Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".



Pixel Array Image Drawing in Window cropping Mode



Drive Timing Chart for Parallel Output in Window cropping Mode



Drive Timing Chart for Serial Output in Window cropping Mode

Description of Various Function

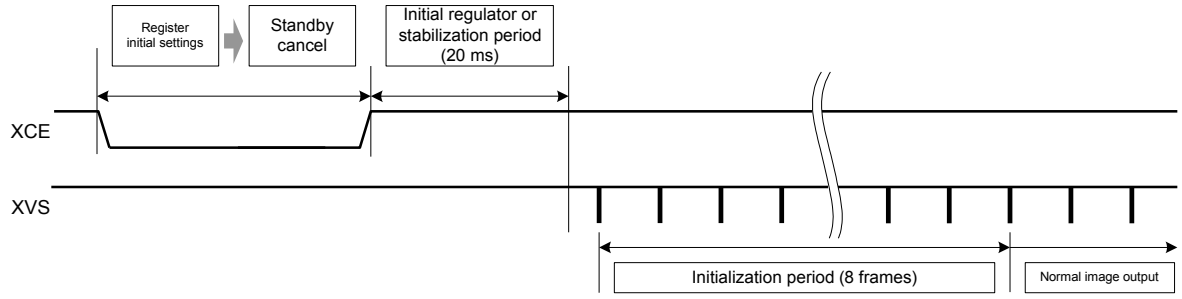
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing "1" to the standby control register STANDBY (address 00h (I^2C: 3000h), Bit [0]).
Standby mode is also established after Power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details (Chip ID = 02h)				Initial value	Setting value	Status	Remarks
	Register	Chip ID	Address ( ): I^2C	bit				
STANDBY	—	02h	00h (3000h)	[0]	1	1	Standby	Register communication is executed even in standby mode
						0	Operating	

The serial communication registers hold the previous values.
However, the address registers transmitted in standby mode are overwritten.
The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to "0".
Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (20 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the DMODE pin. Establish the DMODE pin status before canceling the system reset. (Do not switch this pin status during operation.)

Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal.
See the section of "Operating mode" for the number of output data line and 1H period.

Set the XMSTA register (address 02h (I^2C: 3002h) [0]) to “0” in order to start the operation after setting to master mode.
In addition, set the count number of sync signal in vertical direction by the VMAX [15:0] register (address 18h (I^2C:3 018h) [7:0], 19h (I^2C: 3019h) [7:0]) and the clock number in horizontal direction by the HMAX [15:0] register (address 1Bh (I^2C: 301Bh) [7:0], 1Ch (I^2C: 301Ch) [7:0]). See the description of Operation Mode for details of the section of “Operating Modes”.

Slave and Master Mode Setting

Pin name	Pin processing	Operation mode	Remarks
DMODE pin	Low fixed	Master Mode	High: OVDD Low: GND
	High fixed	Slave Mode	

Registers that Requires Setting in Master Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I^2C	bit			
XMSTA	—	02h (3002h)	[0]	1	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [15:0]	VMAX [7:0]	18h (3018h)	[7:0]	0444h	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	19h (3019h)	[7:0]			
HMAX [15:0]	HMAX [7:0]	1Bh (301Bh)	[7:0]	0CE4h	See the item of each drive mode.	Clock number per line designated
	HMAX [15:8]	1Ch (301Ch)	[7:0]			
XVSLNG [1:0]	XVSLNG [1:0]	46h (3046h)	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS width designated
XHSLNG [1:0]	XHSLNG [1:0]	47h (3047h)	[5:4]	0h	0: Min. to 3: Max. See the next page.	XHS width designated
XVSOUTSEL [1:0]	—	49h (3049h)	[1:0]	0h	0: High level output 2: VSYNC output Others: Setting prohibited	
XHSOUTSEL [1:0]	—		[3:2]	0h	0: High level output 2: HSYNC output Others: Setting prohibited	

Detailed Register Setting of XHSLNG

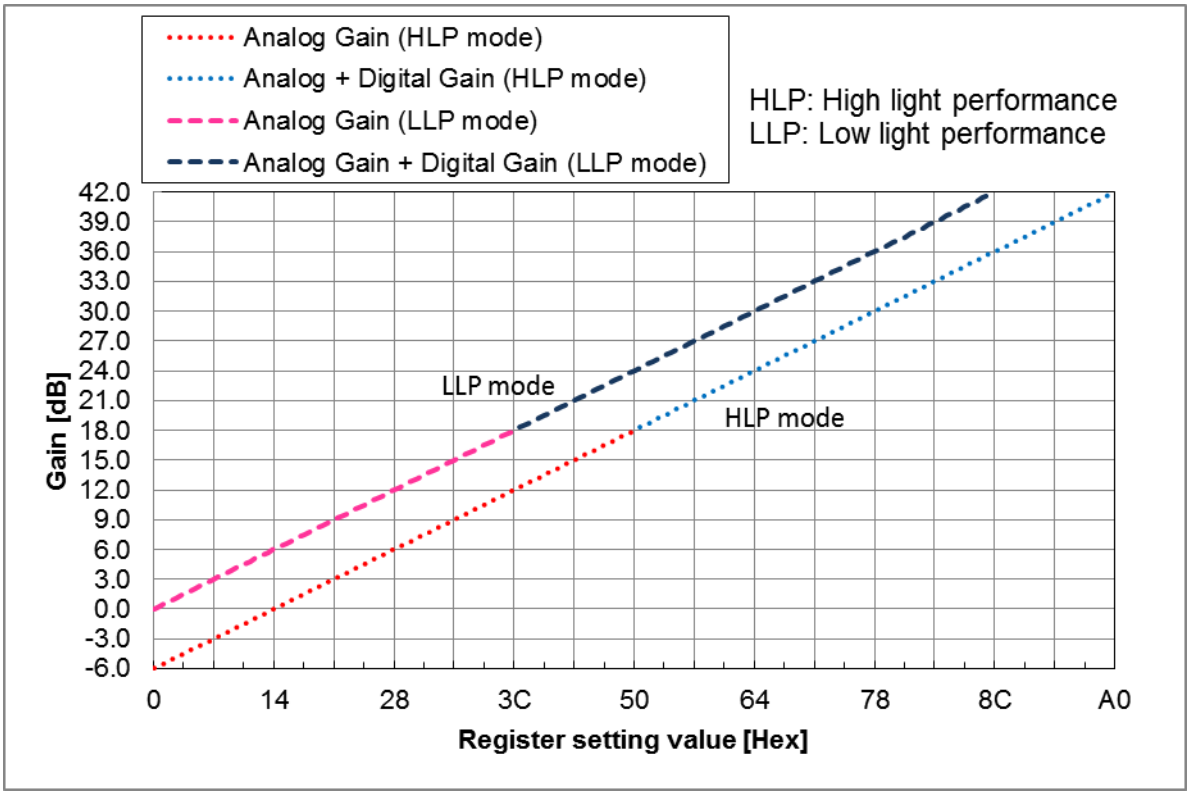
Register name	Setting value	CMOS Parallel / Low-voltage LVDS Parallel (unit: pixels)	Low-voltage LVDS Serial (unit: DCK)		
			1 ch	2 ch	4 ch
XHSLNG [1:0]	0	64	384	192	96
	1	128	768	384	192
	2	256	1536	768	384
	3	512	3072	1536	768

Gain Adjustment Function

PGC Outline

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 42 dB by the GAIN [7:0] register (address 14h (I^2C: 3014h) [7:0]) setting. The same setting is applied in all colors.
In addition, the readout drive mode can be switched to High light performance mode to support imaging under high illumination or Low light performance mode to make much of visibility under low illumination to increase the sensor output level by setting the register LP_MODE [7:0] (address: 11h (I^2C: 3011h) [7:0]).
In standard imaging, setting to Low light performance mode is recommended.

See the List of Gain Setting Register Value for Each Register.



List of PGC Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I^2C	bit		Setting range	
LP_MODE	—	11h (3011sh)	[7:0]	00h	00h	High light Performance mode
					14h	Low light Performance mode (recommend)
GAIN	—	14h (3014h)	[7:0]	00h	00h-8Ch (0d-140d)	See next page.

List of Gain Setting Register Value

Gain [dB]	GAIN [7:0]		Gain [dB]	GAIN [7:0]		Gain [dB]	GAIN [7:0]	
	High light performance mode (LP_MODE = 00h)	Low light performance mode (LP_MODE = 14h)		High light performance mode (LP_MODE = 00h)	Low light performance mode (LP_MODE = 14h)		High light performance mode (LP_MODE = 00h)	Low light performance mode (LP_MODE = 14h)
-6	0h	—	10.2	36h	22h	26.4	6Ch	58h
-5.7	1h	—	10.5	37h	23h	26.7	6Dh	59h
-5.4	2h	—	10.8	38h	24h	27	6Eh	5Ah
-5.1	3h	—	11.1	39h	25h	27.3	6Fh	5Bh
-4.8	4h	—	11.4	3Ah	26h	27.6	70h	5Ch
-4.5	5h	—	11.7	3Bh	27h	27.9	71h	5Dh
-4.2	6h	—	12	3Ch	28h	28.2	72h	5Eh
-3.9	7h	—	12.3	3Dh	29h	28.5	73h	5Fh
-3.6	8h	—	12.6	3Eh	2Ah	28.8	74h	60h
-3.3	9h	—	12.9	3Fh	2Bh	29.1	75h	61h
-3	Ah	—	13.2	40h	2Ch	29.4	76h	62h
-2.7	Bh	—	13.5	41h	2Dh	29.7	77h	63h
-2.4	Ch	—	13.8	42h	2Eh	30	78h	64h
-2.1	Dh	—	14.1	43h	2Fh	30.3	79h	65h
-1.8	Eh	—	14.4	44h	30h	30.6	7Ah	66h
-1.5	Fh	—	14.7	45h	31h	30.9	7Bh	67h
-1.2	10h	—	15	46h	32h	31.2	7Ch	68h
-0.9	11h	—	15.3	47h	33h	31.5	7Dh	69h
-0.6	12h	—	15.6	48h	34h	31.8	7Eh	6Ah
-0.3	13h	—	15.9	49h	35h	32.1	7Fh	6Bh
0	14h	0h	16.2	4Ah	36h	32.4	80h	6Ch
0.3	15h	1h	16.5	4Bh	37h	32.7	81h	6Dh
0.6	16h	2h	16.8	4Ch	38h	33	82h	6Eh
0.9	17h	3h	17.1	4Dh	39h	33.3	83h	6Fh
1.2	18h	4h	17.4	4Eh	3Ah	33.6	84h	70h
1.5	19h	5h	17.7	4Fh	3Bh	33.9	85h	71h
1.8	1Ah	6h	18	50h	3Ch	34.2	86h	72h
2.1	1Bh	7h	18.3	51h	3Dh	34.5	87h	73h
2.4	1Ch	8h	18.6	52h	3Eh	34.8	88h	74h
2.7	1Dh	9h	18.9	53h	3Fh	35.1	89h	75h
3	1Eh	Ah	19.2	54h	40h	35.4	8Ah	76h
3.3	1Fh	Bh	19.5	55h	41h	35.7	8Bh	77h
3.6	20h	Ch	19.8	56h	42h	36	8Ch	78h
3.9	21h	Dh	20.1	57h	43h	36.3	8Dh	79h
4.2	22h	Eh	20.4	58h	44h	36.6	8Eh	7Ah
4.5	23h	Fh	20.7	59h	45h	36.9	8Fh	7Bh
4.8	24h	10h	21	5Ah	46h	37.2	90h	7Ch
5.1	25h	11h	21.3	5Bh	47h	37.5	91h	7Dh
5.4	26h	12h	21.6	5Ch	48h	37.8	92h	7Eh
5.7	27h	13h	21.9	5Dh	49h	38.1	93h	7Fh
6	28h	14h	22.2	5Eh	4Ah	38.4	94h	80h
6.3	29h	15h	22.5	5Fh	4Bh	38.7	95h	81h
6.6	2Ah	16h	22.8	60h	4Ch	39	96h	82h
6.9	2Bh	17h	23.1	61h	4Dh	39.3	97h	83h
7.2	2Ch	18h	23.4	62h	4Eh	39.6	98h	84h
7.5	2Dh	19h	23.7	63h	4Fh	39.9	99h	85h
7.8	2Eh	1Ah	24	64h	50h	40.2	9Ah	86h
8.1	2Fh	1Bh	24.3	65h	51h	40.5	9Bh	87h
8.4	30h	1Ch	24.6	66h	52h	40.8	9Ch	88h
8.7	31h	1Dh	24.9	67h	53h	41.1	9Dh	89h
9	32h	1Eh	25.2	68h	54h	41.4	9Eh	8Ah
9.3	33h	1Fh	25.5	69h	55h	41.7	9Fh	8Bh
9.6	34h	20h	25.8	6Ah	56h	42	A0h	8Ch
9.9	35h	21h	26.1	6Bh	57h			

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [8:0] register (address: 0Ah (I^2C: 300Ah) [7:0], 0Bh (I^2C: 300Bh) [0]). When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

* Use with values shown below is recommended.
  12-bit output: 0F0h (240d)

List of Black Level Adjustment Register

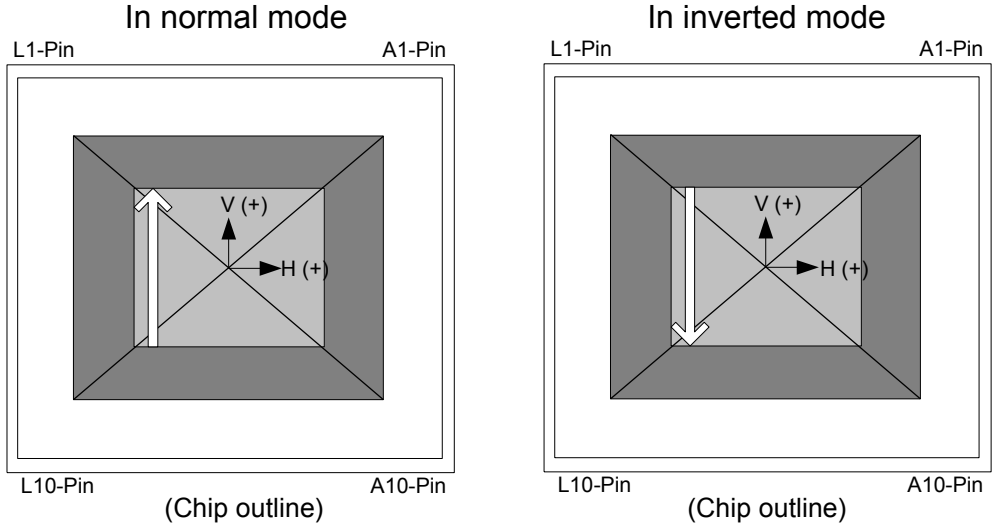
Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
BLKLEVEL [8:0]	BLKLEVEL [7:0]	0Ah (300Ah)	[7:0]	03Ch	000h to 1FFh
	BLKLEVEL [8]	0Bh (300Bh)	[0]		

Vertical Normal Operation and Inverted Drive

The sensor readout direction (normal / inverted) in vertical direction can be switched by the VREVERSE (address 07h (I^2C: 3007h) [0]) register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Vertical Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
VREVERSE	—	07h (3007h)	[0]	0h	0: Normal (Initial value) 1: Inverted



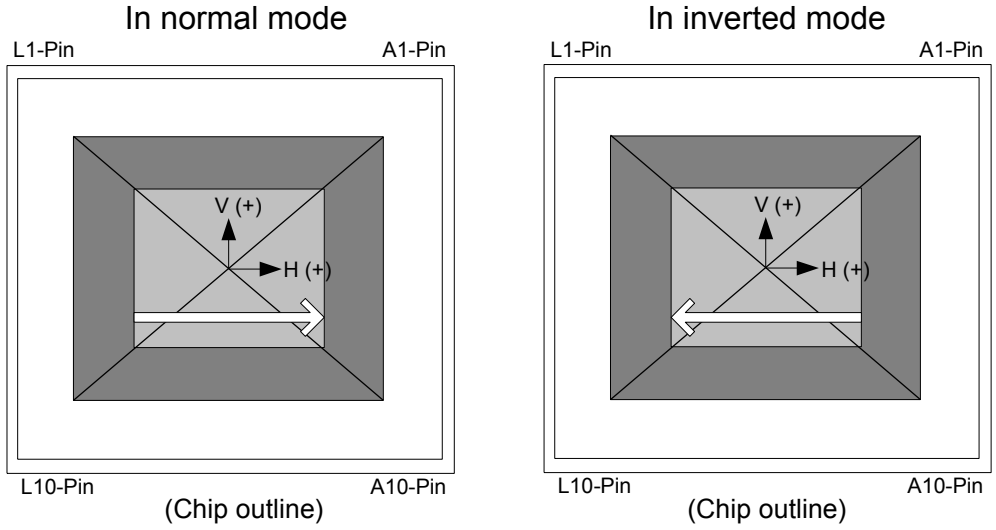
Normal and Inverted Drive Outline in Vertical Direction

Horizontal Normal Operation and Inverted Drive

The sensor readout direction (normal / inverted) in vertical direction can be switched by the HREVERSE (address 07h (I^2C: 3007h) [1]) register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes.

List of Horizontal Drive Direction Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
HREVERSE	—	07h (3007h)	[1]	0h	0: Normal (Initial value) 1: Inverted



Normal and Inverted Drive Outline in Horizontal Direction

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1 + 1) × (1H period) + t_{OFFSET}

Note) 1. The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
2. See “Operating Modes” for the 1H period.
3. t_{OFFSET} is 3.92 [µs] .

In this item, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

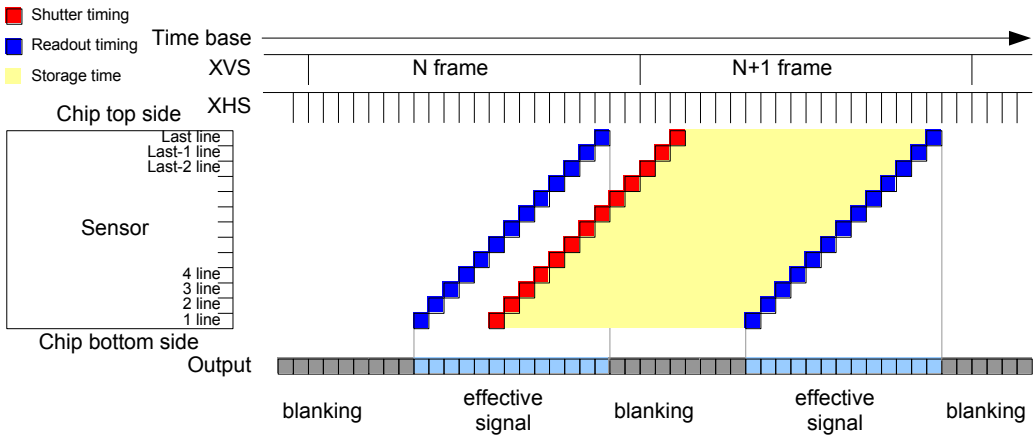


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 [15:0] register (address: 20h (I^2C: 3020h) [7:0], 21h (I^2C: 3021h) [7:0]).

Set SHS1 [15:0] to a value between 0 and (Number of lines per frame - 2). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX [15:0] register (address: 18h (I^2C: 3018h) [7:0], 19h (I^2C: 3019h) [7:0]).
The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
SHS1 [15:0]	SHS1 [7:0]	20h (3020h)	[7:0]	00000h	Set the shutter sweep time. 0 to (Number of lines per frame - 2) * (Number of lines per frame - 1) : Setting prohibited
	SHS1 [15:8]	21h (3021h)	[7:0]		
VMAX [15:0]	VMAX [7:0]	18h (3018h)	[7:0]	00444h	Set the number of lines per frame (only in master mode) See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	19h (3019h)	[7:0]		

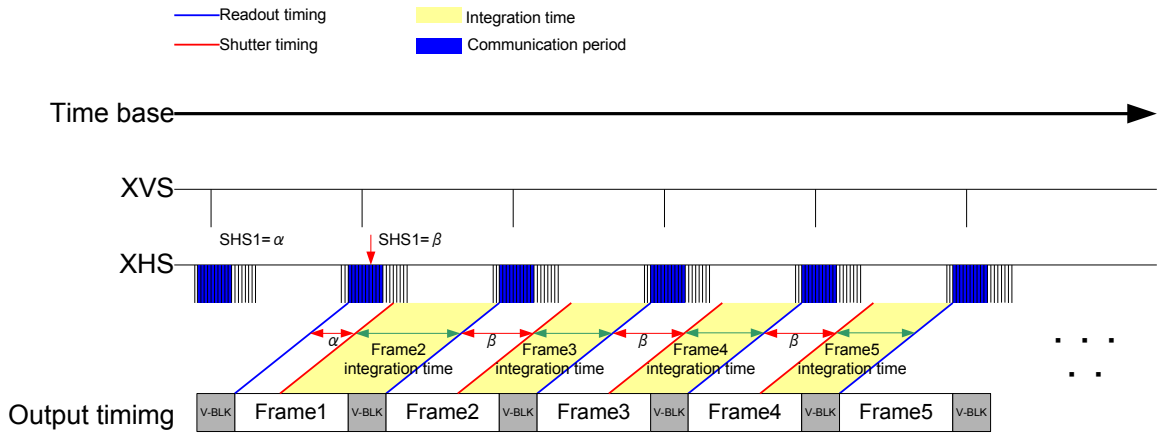


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [15:0] (address: 18h (I^2C: 3018h) [7:0], 19h (I^2C: 3019h) [7:0]) value compared to normal operation.
When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

The maximum VMAX value is 65535d, and the maximum SHS1 value is 65533d. When the number of lines per frame is set to the maximum value, the integration time in all-pixel scan mode at 60 frame/s is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

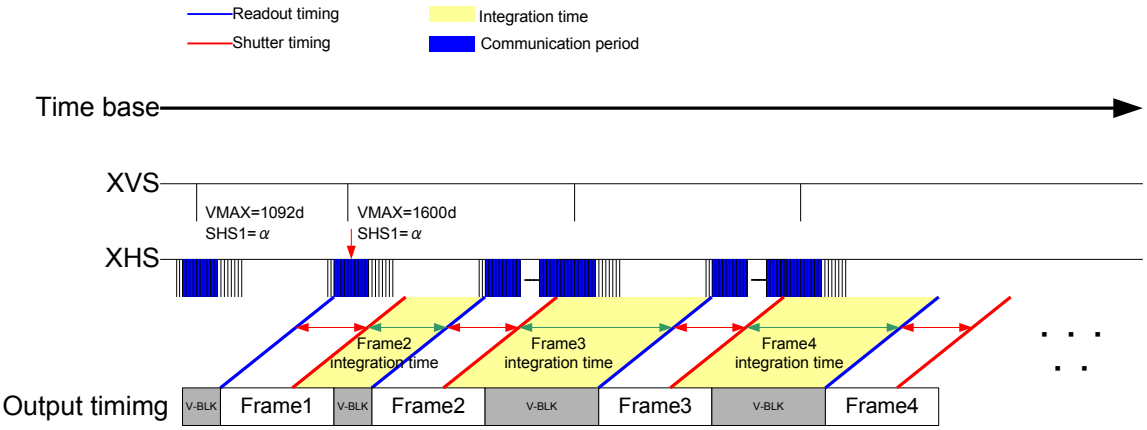


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Setting (in all-pixel mode at 59.94 frame/s)

Operation	Sensor setting (register)		Integration time
	VMAX*	SHS1**	
Normal frame rate	1092	1090	1H + t_{OFFSET}
		⋮	⋮
		N	(1092 - (N + 1)) H + t_{OFFSET}
		⋮	⋮
		1	1090H + t_{OFFSET}
		0	1091H + t_{OFFSET}
Long-time exposure operation	M	N	(M - (N + 1)) H + t_{OFFSET}

* In sensor master mode. In slave mode, the interval is same as XVS input.
** The SHS1 setting value (N) is set between “0” and “the VMAX value (M) – 2”.

Signal Output

Output Pin Settings

The output formats of this sensor support the following modes.

CMOS logic parallel SDR output
Low voltage LVDS parallel DDR output
Low voltage LVDS serial (1 ch / 2 ch / 4 ch switching) DDR output

Each mode is set using the register OPORTSEL [3:0] (Address: 44h (I^2C: 3044h) [7:4]). The table below shows the output format settings.

Settings for Output Format

Register name	Register details (Chip ID = 02h)		Initial value	Setting value	Description
	Address ( ) : I^2C	bit			
OPORTSEL [3:0]	44h (3044h)	[7:4]	0h	0h	CMOS logic parallel SDR output
				6h	Low voltage LVDS parallel DDR output
				Ch	Low voltage LVDS serial 1 ch DDR output
				Dh	Low voltage LVDS serial 2 ch DDR output
				Eh	Low voltage LVDS serial 4 ch DDR output

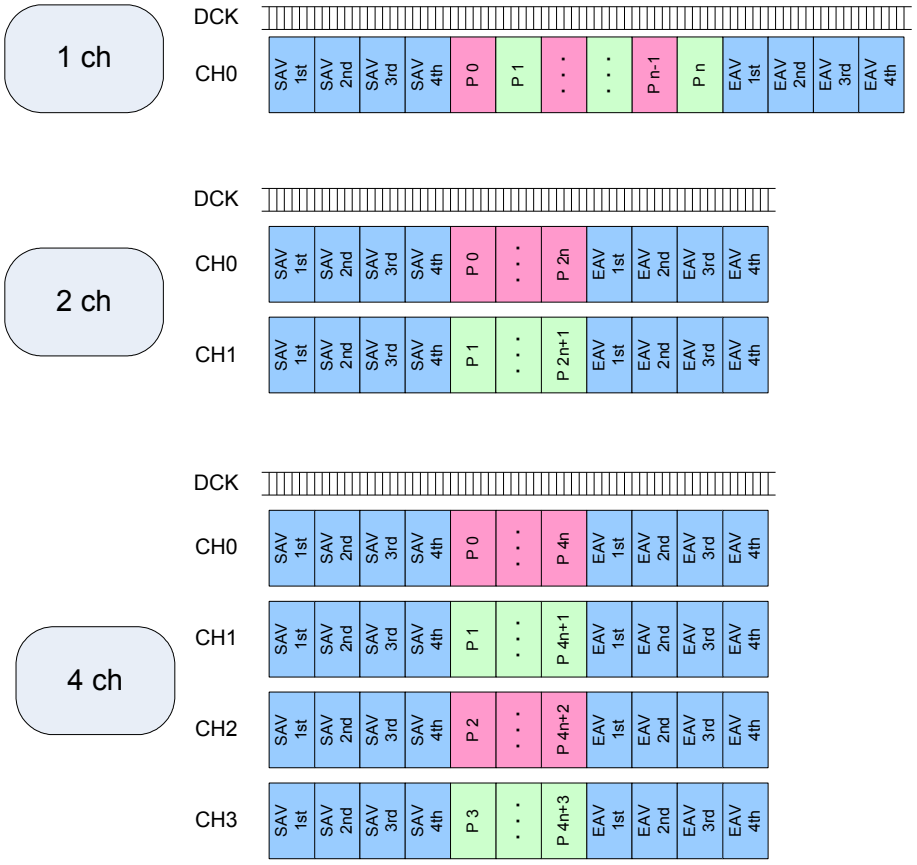
* In CMOS output mode, Clock is output from DCKP pin. DCKM pin is fixed to low level.
* In CMOS output mode, Data are output from DOP [11:0] pins. DOM [11:0] pins fixed to low level.

Each output pin is shown in the table below when setting low-voltage LVDS serial 1 ch / 2 ch / 4 ch output.

Output Pins for Low voltage LVDS Serial mode

DOP / DOM	Low voltage LVDS serial DDR output		
	1 ch	2 ch	4 ch
DOP11 to 8 / DOM11 to 8	Hi-Z	Hi-Z	Hi-Z
DOP7 / DOM7	Hi-Z	Hi-Z	CH3
DOP6 / DOM6	Hi-Z	CH1	CH1
DOP5 / DOM5	CH0	CH0	CH0
DOP4 / DOM4	Hi-Z	Hi-Z	CH2
DOP3 to 0 / DOM3 to 0	Hi-Z	Hi-Z	Hi-Z

Low-voltage LVDS serial 1 ch / 2 ch / 4 ch output format is shown in the figure below.
When setting 1 ch, pixel data is output in order after four data of SAV is output, and then four data of EAV is output to CH0.
When setting 2 ch, after four data of SAV is output in the order of CH0 and CH1 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH0 and CH1 respectively.
When setting 4 ch, after four data of SAV is output in the order of CH0, CH1, CH2 and CH3 pixel data is repeatedly output in the same order and then four data of EAV is output in the same order to CH0, CH1, CH2 and CH3 respectively.
Data is sent MSB first.
For details, see drive timing in each mode in the section of "Operation Mode".



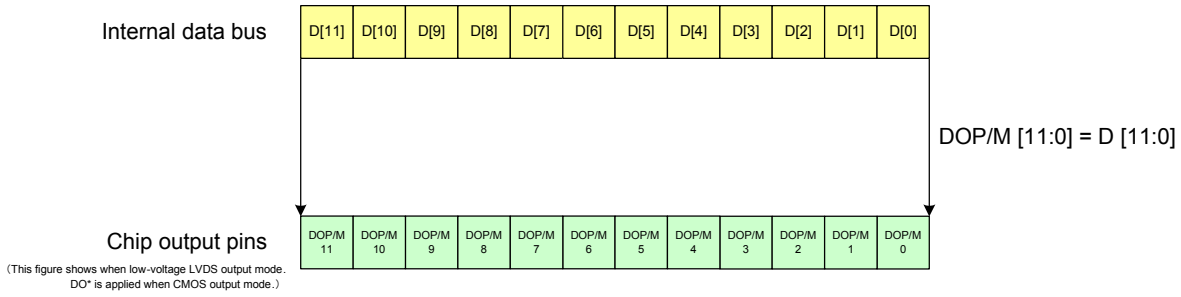
Output Format of Low voltage LVDS Serial 1 ch / 2 ch / 4 ch

Output Pin Bit Assignments

When low-voltage LVDS parallel output mode, data is output to the DOP [11:0] and DOM [11:0].
When CMOS parallel output, data is output to the DOP [11:0], or the DOM [11:0] is fixed to low level.
When low-voltage LVDS serial output, continuous data is output MSB first by 12-bit output.

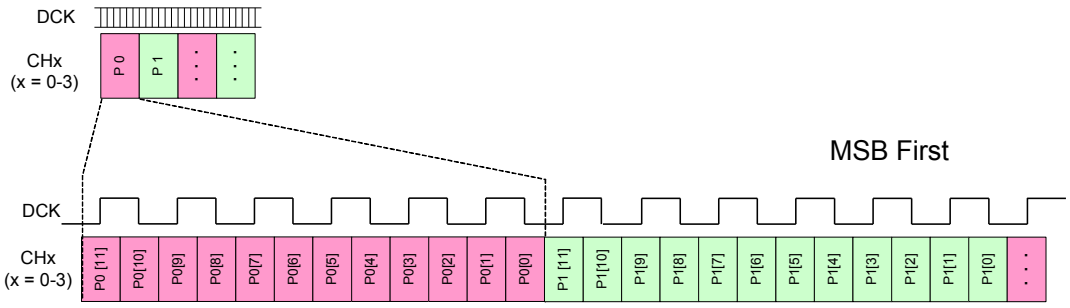
(Low-voltage LVDS parallel 12-bit output or CMOS parallel 12-bit output)

The lower 12 bits of the internal data bus are output on the chip output pins DO.



Bit Assignments in Parallel 12-bit Output

(Low-voltage LVDS serial 12-bit output)



Example of Data format in low-voltage LVDS Serial 12-bit Output

Output Rate Setting

The sensor output rate is determined uniformly by the sensor operating mode and the output format. See the section of “Operating Modes” for the relationship between each setting and the frame rate, data rate and data bit rate.
The registers related to mode setting are shown in the table below.

Related Registers for Setting Operation Mode

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ): I^2C	bit		
WINMODE [1:0]	—	07h (3007h)	[5:4]	0h	0: All-pix scan mode 1: 720p-HD mode 2: Window cropping mode (from all-pix scan mode) 3: Window cropping mode (from 720p mode)
FRSEL [1:0]	—	09h (3009h	[1:0]	2h	1: 60 fps mode 2: 30 fps mode 0,3: Setting prohibited

Output Signal Range

The sensor output has either a 12-bit gradation, but output is not performed over the full range, and the maximum output value is the (FFFh -1) value (12-bit output).
When serial output, the minimum value is 001h. The output range for each output gradation is shown in the table below.
See the item of “Sync Codes” in the section of “Operating Modes” for the sync codes.

Output Gradation and Output Range

Output gradation	Output value		
	Min.		Max.
	Parallel output	Serial output	
12 bit	000h	001h	FFEh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 27 MHz or 54 MHz or 37.125 MHz or 74.25 MHz for INCK frequency. The value according to the combination of input INCK and output format is set to register INCKSEL1, INCKSEL2 and INCKSEL3. The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value	Remarks
	Register	Address ( ) : I^2C	bit			
INCKSEL1	—	5Bh (305Bh)	[0]	1h	0: Input 37.125 MHz or 74.25 MHz 1: Input 27 MHz or 54 MHz	
INCKSEL2	—	5Dh (305Dh)	[4]	1h	0: Input 27 MHz or 37.125 MHz 1: Input 54 MHz or 74.25 MHz	
INCKSEL3	—	5Fh (305Fh)	[4]	1h	0: Input 27 MHz 1: Input 54 MHz	When INCK input frequency is 37.125 MHz or 74.25 MHz, this setting is invalid.

List of INCK Setting

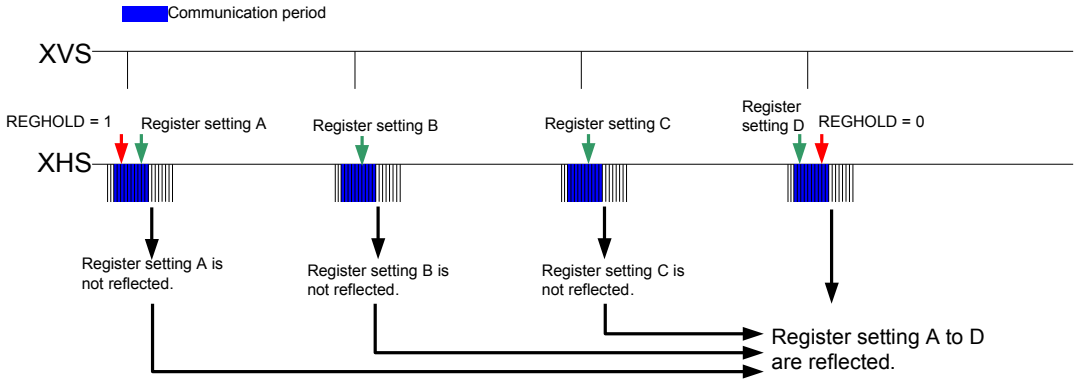
INCK [MHz]	Setting value		
	INCKSEL1	INCKSEL2	INCKSEL3
27	1h	0h	0h
54		1h	1h
37.125	0h	0h	—
74.25		1h	—

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD (address: 01h (I^2C: 3001h) [0]). Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
REGHOLD	—	01h (3001h)	[0]	0h	0: Invalid 1: Valid (register hold)



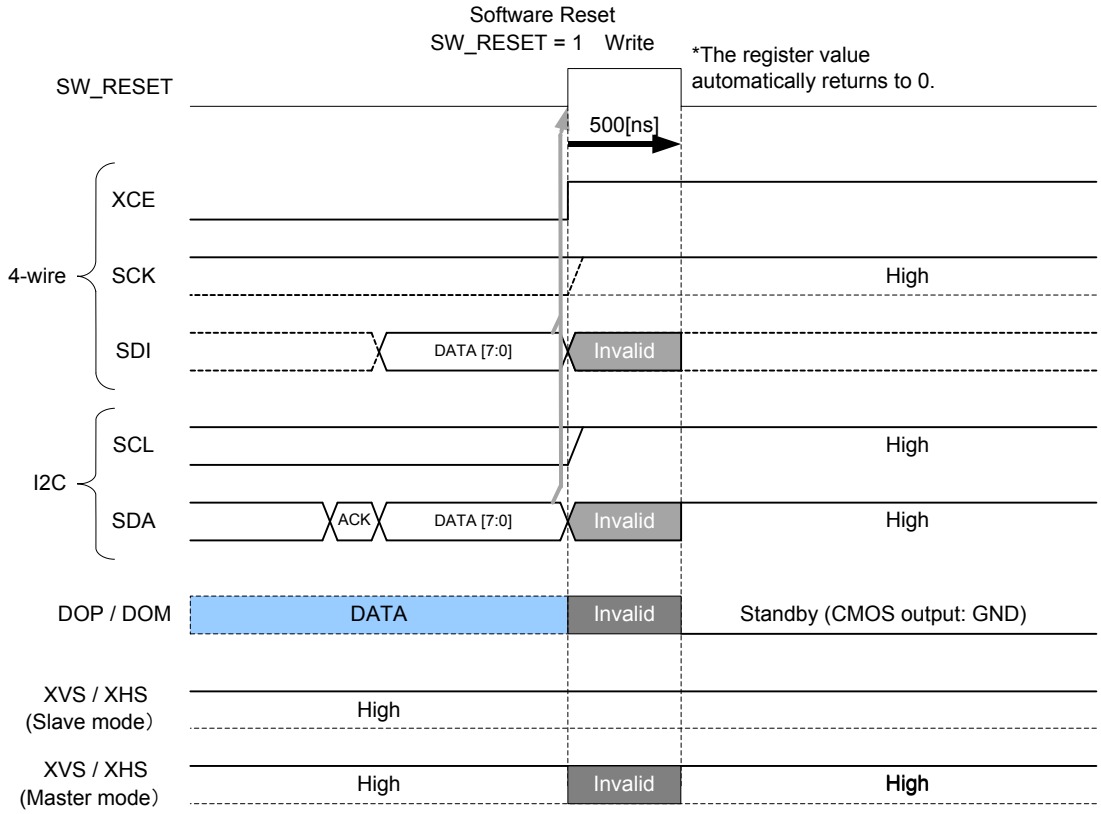
Register Hold Setting

Software Reset

Software reset can be performed by register setting using the register SW_RESET (address: 03h (I^2C: 3003h) [0]). However, the communication to continuous address can not use. In I^2C communication, sensor not return ACK when SW_RESET is transferred.
Sensor reset is performed by setting SW_RESET = 1.
The registers become initial state and standby 500 ns after setting SW_RESET = 1.
The SW_RESET signal returns to "0" automatically.
DOP0 to DOP11, DOM0 to DOM11, DCKP and DCKM become standby (GND) in CMOS output.
The XVS and XHS output High in master mode.
Input High to the XVS and XHS before setting SW_RESET = 1 in slave mode.
Follow the sequence in the item of "Standby Mode" to perform register initial setting and standby cancel from standby state.

Software Reset Register Setting

Register name	Register details (Chip ID = 02h)			Initial value	Setting value
	Register	Address ( ) : I^2C	bit		
SW_RESET	—	03h (3003h)	[0]	0h	0: Normal operation 1: Reset



Software Reset

Mode Transitions

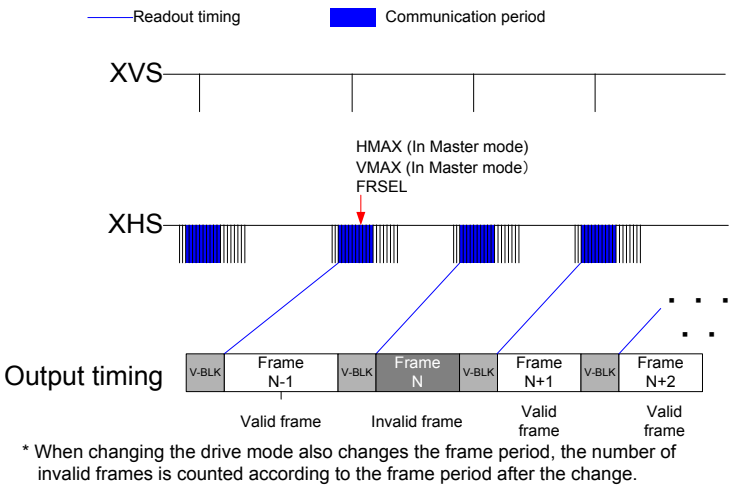
When changing the operating mode during sensor drive operation, first set the sensor to all-pixel scan mode, and then it again to the desired operating mode.
An invalid frame is generated during mode transition.
An invalid frame is generated as well as when changing frame rate in the same operating mode.
The table below shows the number of invalid frames generated by transition between the various modes.
Data is output from sensor during the invalid frame period, but the output values may reflect the integration time or may not be uniform on the screen, or a partially saturated image may be output.

In addition, especially when INCK frequency (register INCKSEL1, INCKSEL2 and INCKSEL3) or output format (register OPORTSEL [3:0]) is changed, transition of the operating mode must be done via sensor standby. When INCK frequency is changed, care should be taken not to be input pulses whose width is shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change.
If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

Number of Invalid Frames Generated during Mode Transitions

Mode transition			Number of invalid frames
All-pixel scan mode	→	720p-HD mode	1
All-pixel scan mode	→	Window cropping mode	
720p-HD mode	→	All-pixel scan mode	
Window cropping mode	→	All-pixel scan mode	
All-pixel scan mode 720p-HD mode	→	Same operation mode Frame rate change (Note 1)	

(Note 1) Excluded when changing input INCK frequency or the register OPORTSEL [3:0].



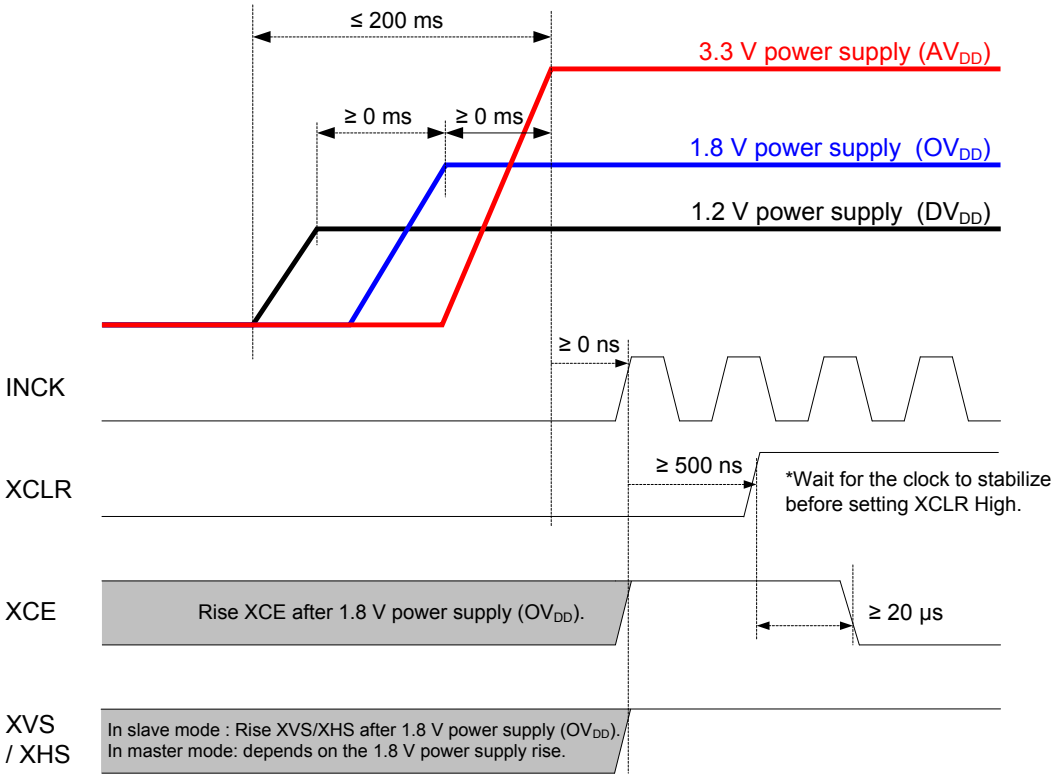
* When changing the drive mode also changes the frame period, the number of invalid frames is counted according to the frame period after the change.

Power-on and Power-off Sequences

Power-on Sequence

Follow the sequence below to turn on the power supplies.

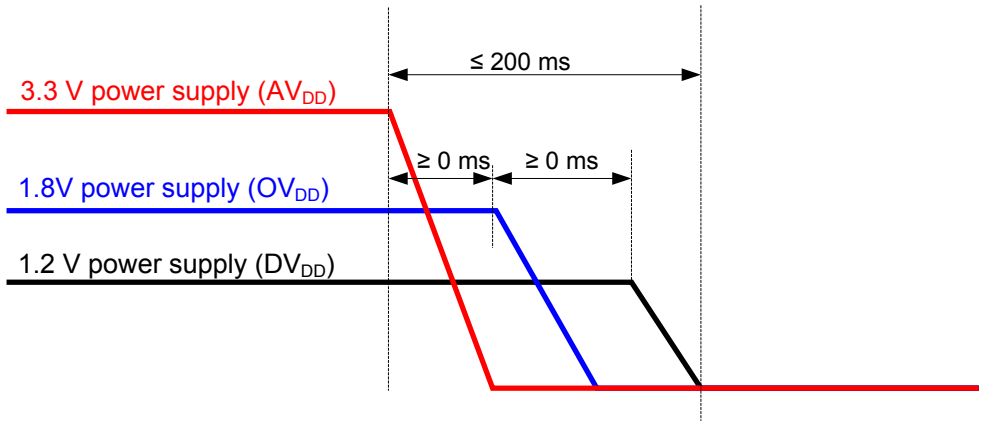
(1) Turn on the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
(2) Start master clock (INCK) input after turning on the power supplies.
(3) The register values are undefined just after Power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
(4) The system clear is applied by setting XCLR to High level. However, the master clock needs to stabilize before setting the XCLR pin to High level.
(5) Make the sensor setting by register communication after the system clear. In case of 4-wired serial control, a period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In case of I^2C serial control, XCE is fixed to High level.



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, DMODE, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.

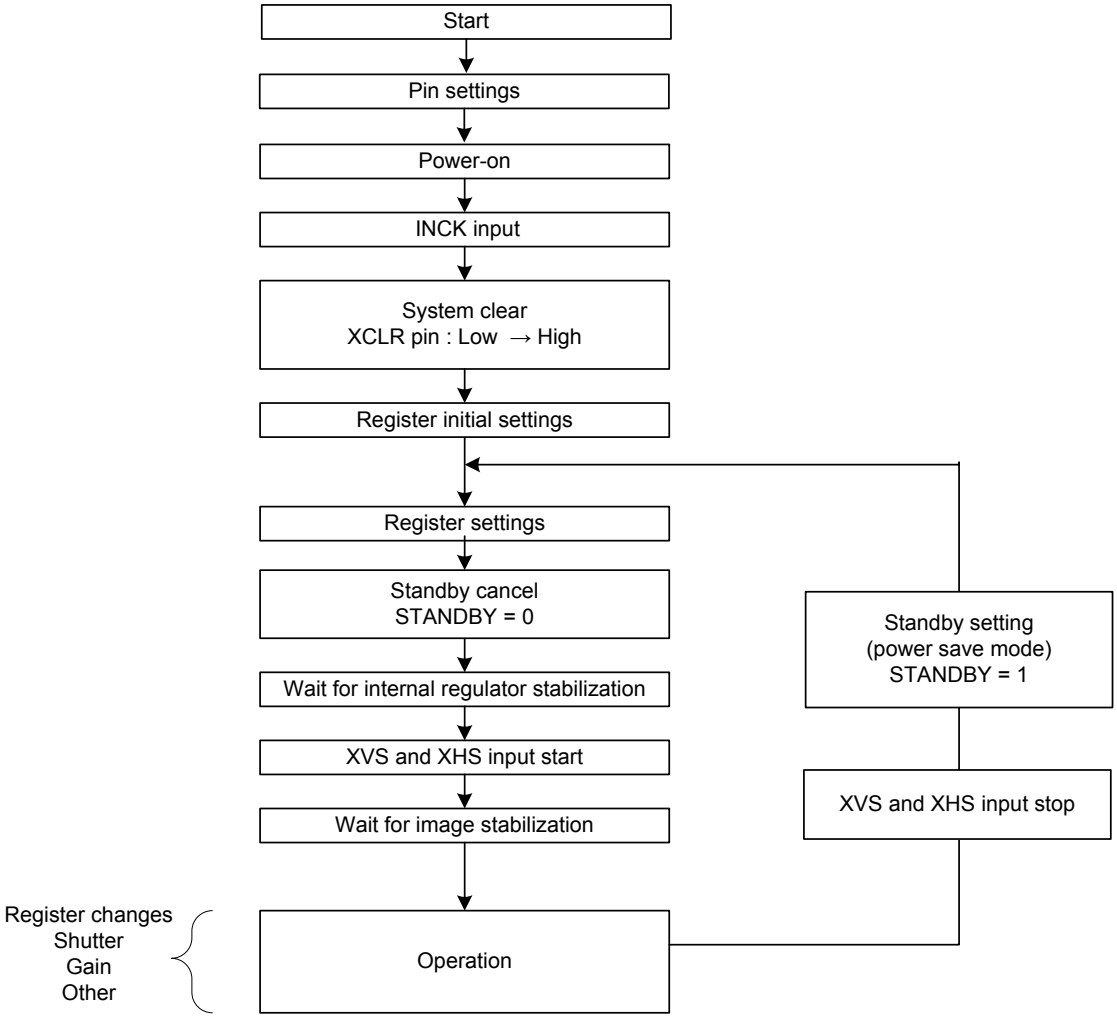


Power –off Sequence

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

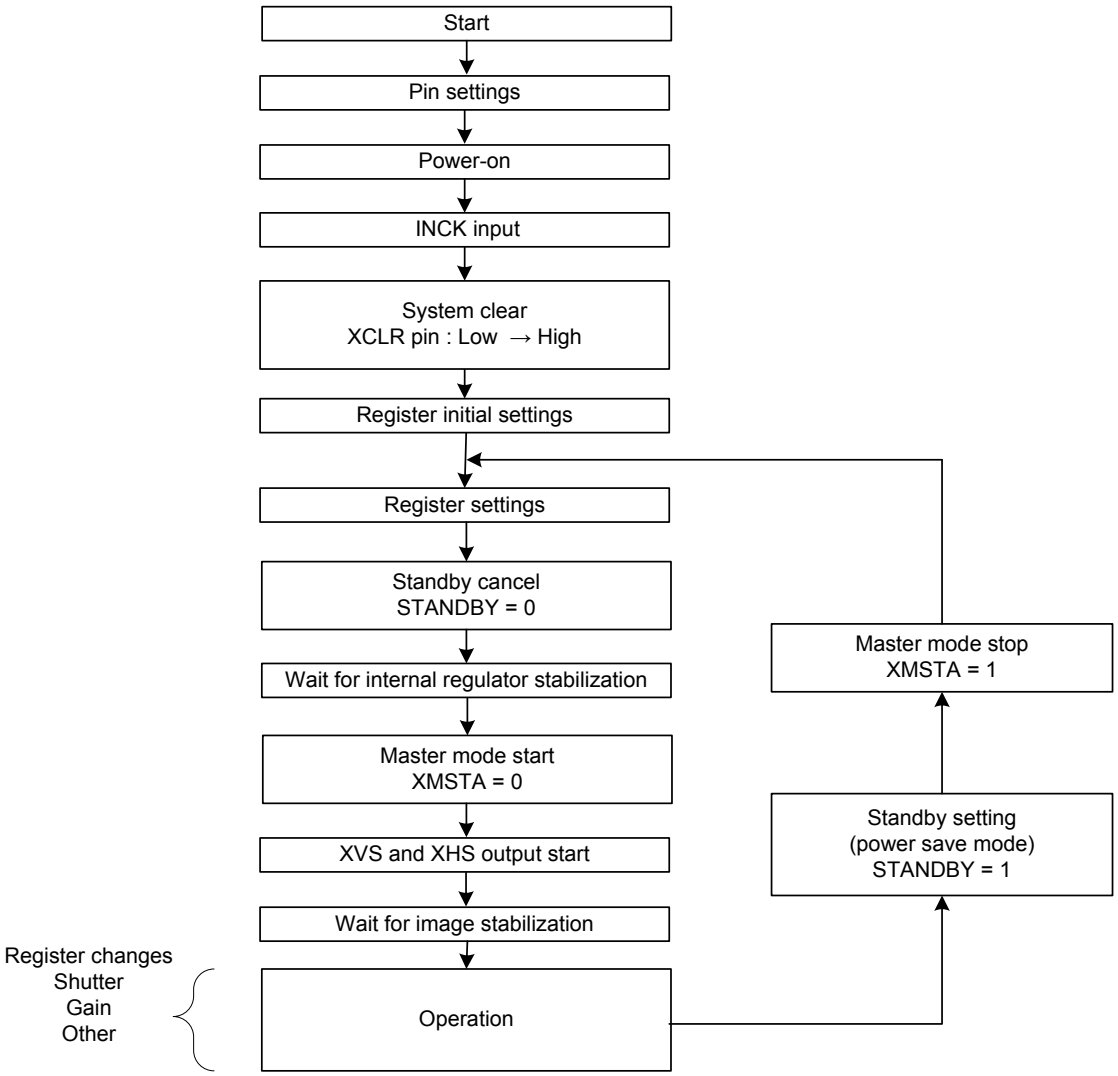
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section.
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

Setting Flow in Sensor Master Mode

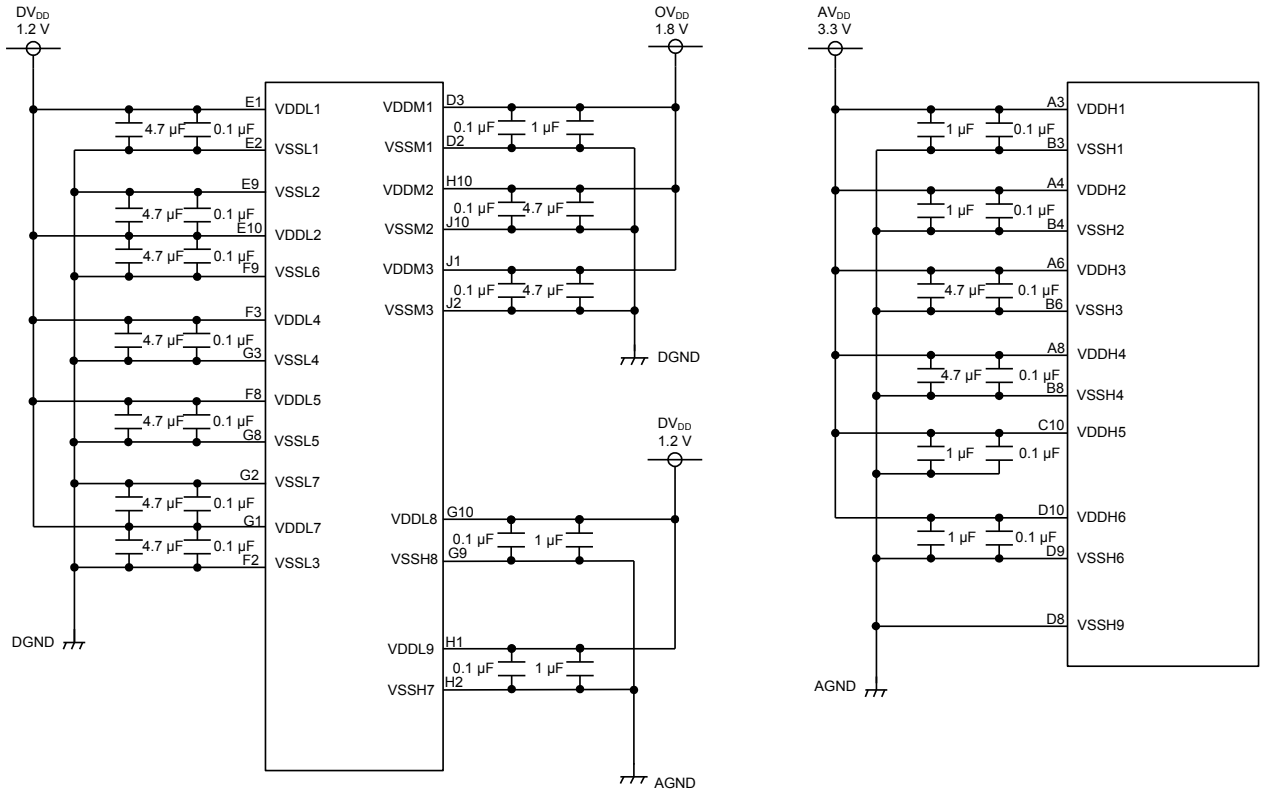
The figure below shows operating flow in sensor slave mode.
For details of "Power on" to "Reset cancel", see the item of "Power on sequence" in this section.
In master mode, “Master mode start” by setting the master mode start register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

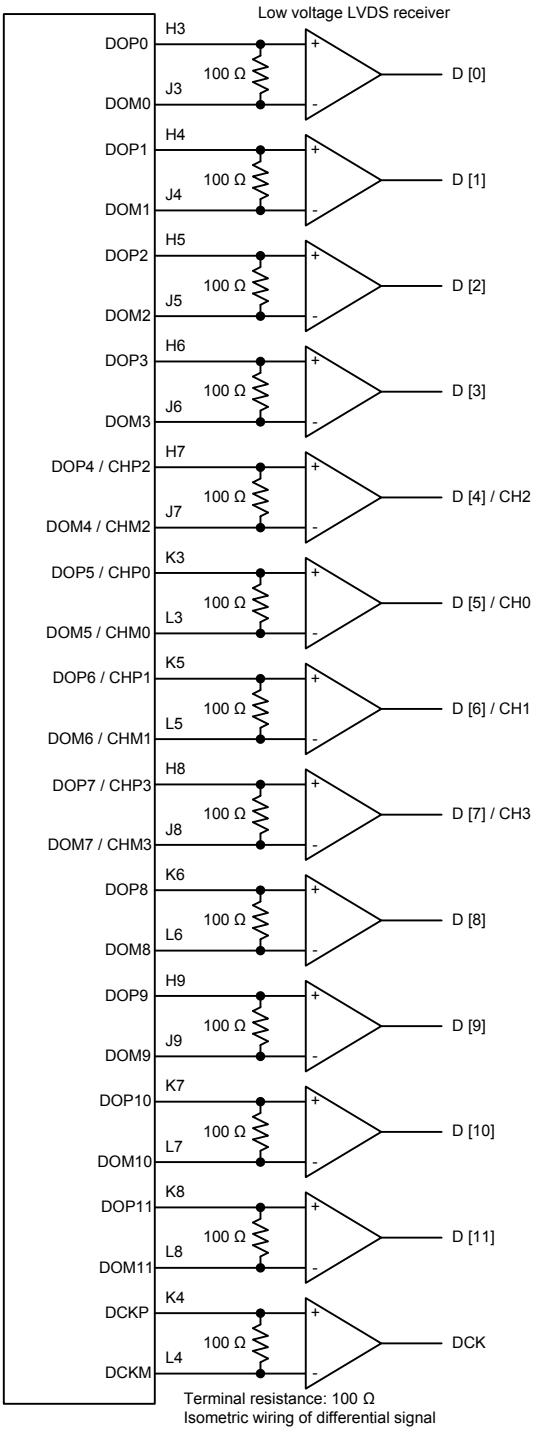
Peripheral Circuit

Power Pins

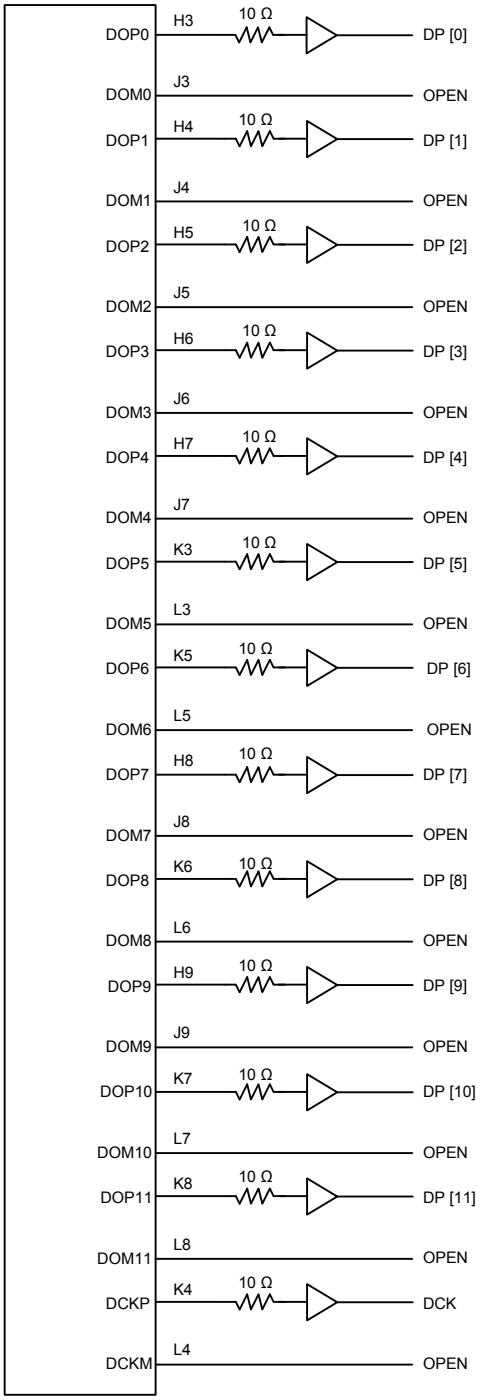


Output Pins

Low voltage LVDS output

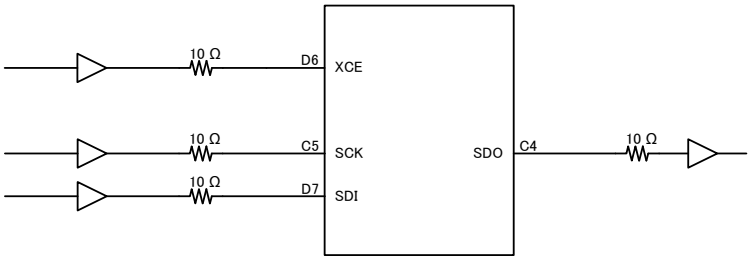


CMOS Logic output

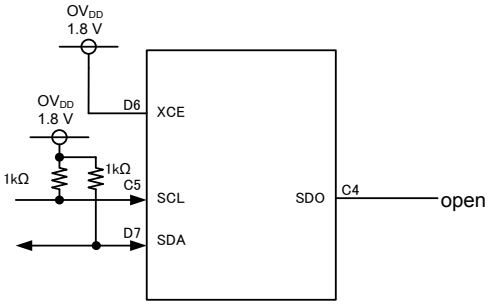


Serial Communication Pins

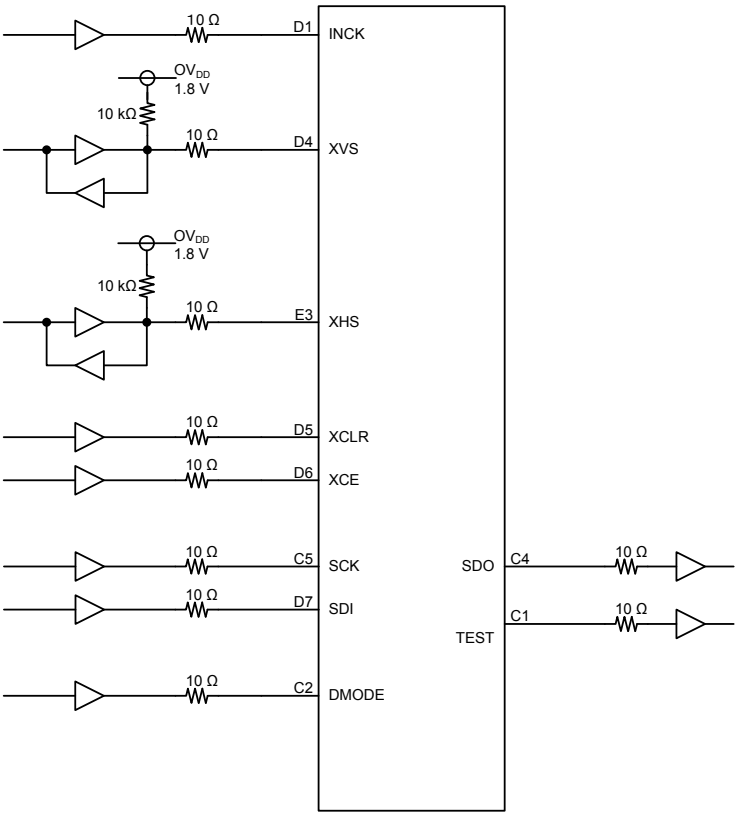
4-wire serial communication

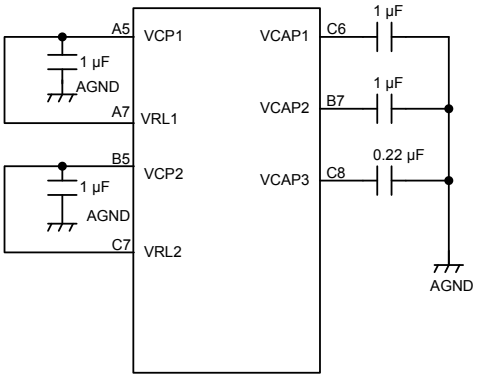


I^2C serial communication



Other Pins





Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

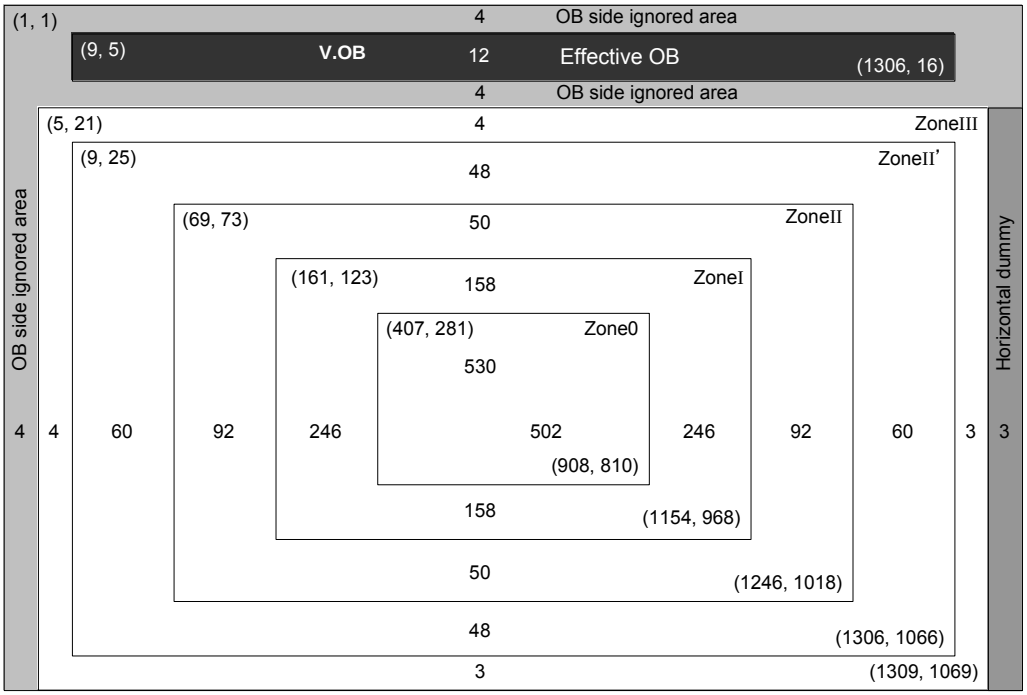
Spot Pixel Specifications

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: -6 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	TBD	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	TBD		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ TBD mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of storage time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	TBD pcs
10.0 mV or higher	TBD pcs
24.0 mV or higher	TBD pcs
50.0 mV or higher	TBD pcs
72.0 mV or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

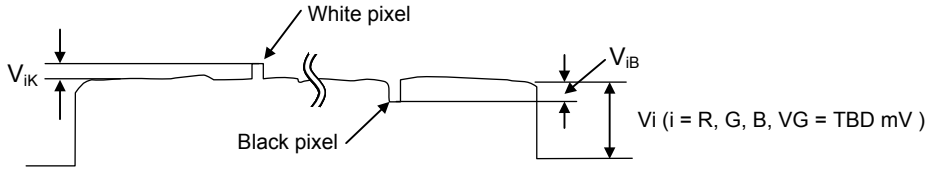
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is TBD mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

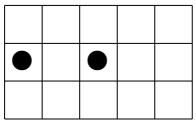
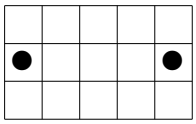
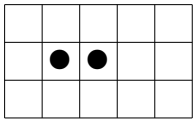
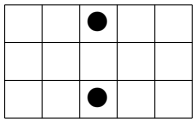
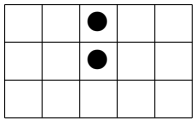
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

Signal output waveform of R / G / B channel

Spot Pixel Pattern Specifications

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

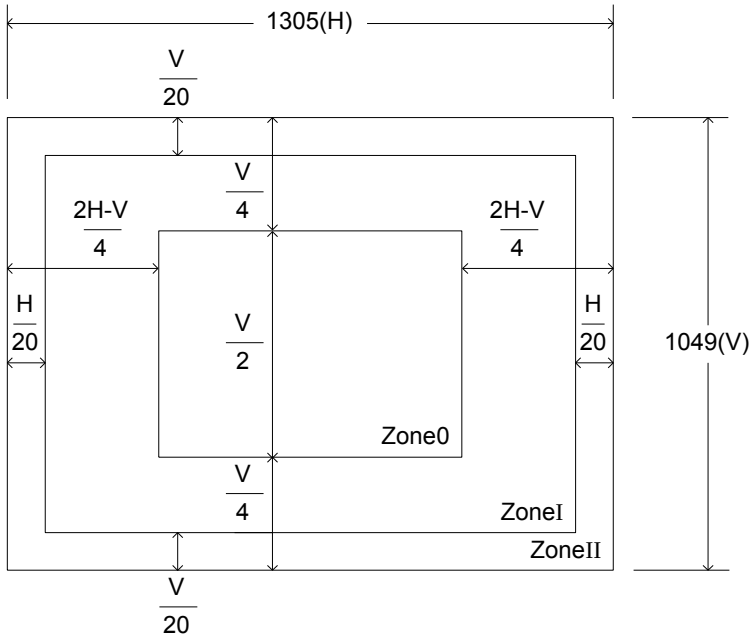
No.	Pattern (R G / G B: Specified in the left pixel array)	White pixel	Black pixel	Bright pixel
1	 Same color	Rejected	Rejected	Rejected
2	 Same color	Rejected	Rejected	Rejected
3	 Different color	Allowed	Allowed	Allowed
4	 Same color	Rejected	Allowed	Allowed
5	 Different color	Allowed	Allowed	Allowed

Note) 1. "● " shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated "Rejected" is selected and removed.
3. Spot pixels indicated "Allowed" are not the subject of selected rejection. They are counted including the number of allowable spot pixels by zone.
4. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Stain Specifications

Zone	Allowable pixels	Size	Level	Lens aperture
0 to II	0	L ≥ 3	R ≥ 8 %	F = 16
Means no stain over three lines or more.				

Stain Zone Definition

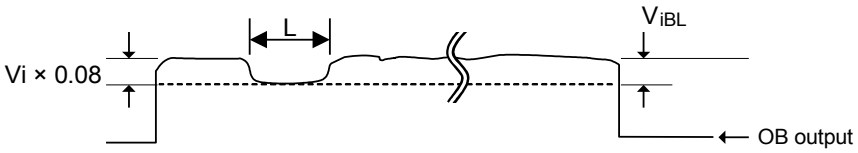


Stain Measurement Method

In the following measurement, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the G channel signal output is 960 mV. Measure the local dip in the average value of the R / G / B channel signal output (Vi_{BL}), and then calculate the stain level (R) as the ratio of Vi_{BL} to the average value of the R / G / B channel signal output (Vi).

Stain level R = (Vi_{BL} / Vi) × 100 [%] (i = R, G, B)

At the same time, the size (L) of the area where the stain level is 8 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.



Signal output waveform of R / G / B channel

Marking (TBD)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

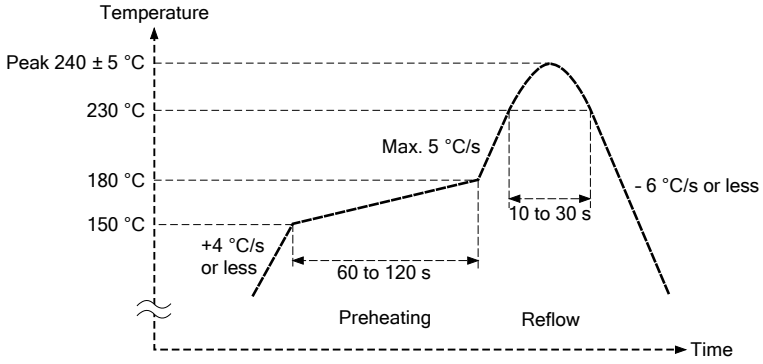
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

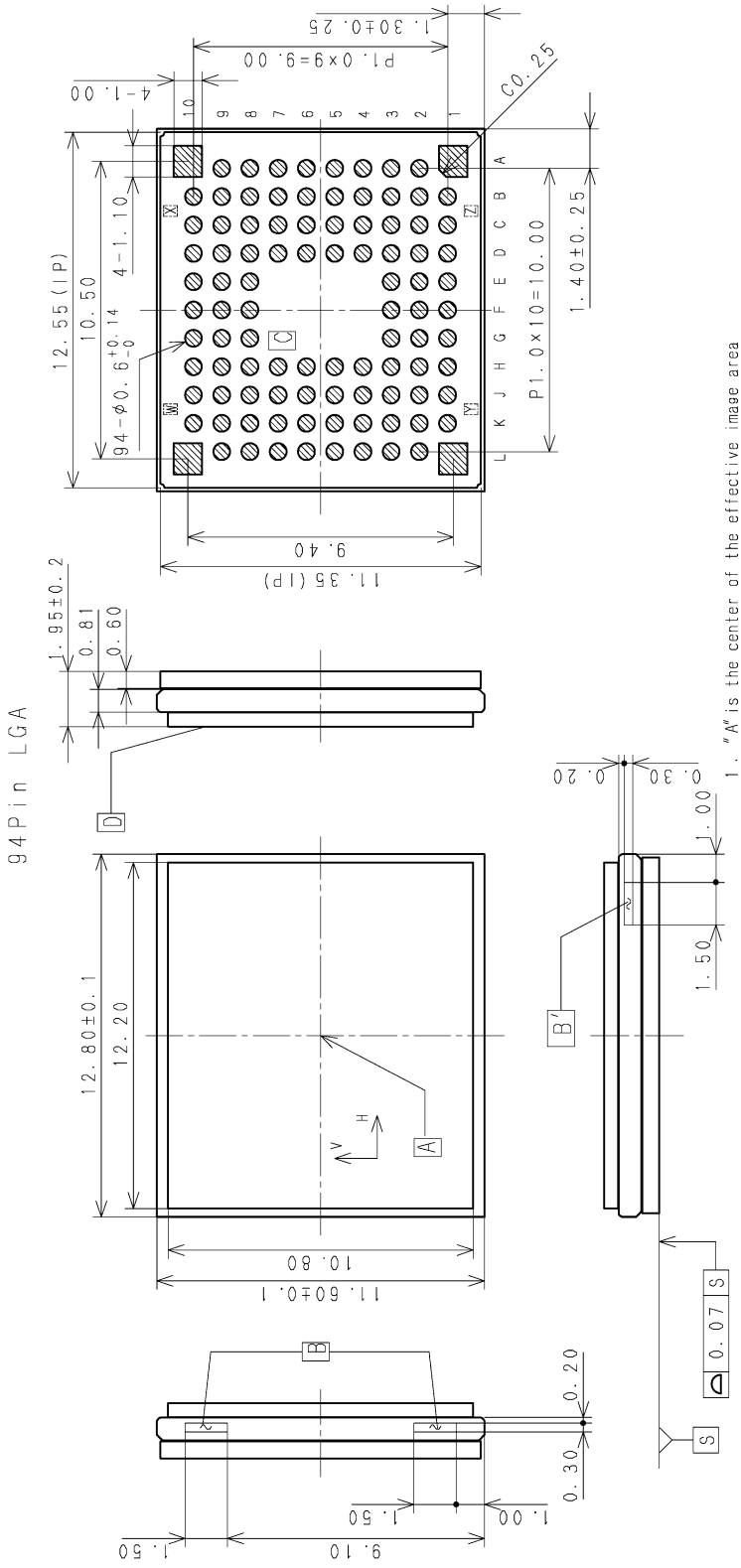
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit: mm)



1. "A" is the center of the effective image area
2. The two points"B"of the package are the horizontal reference
3. The point"B'"of the package is the vertical reference
4. The bottom"C"of the package is the height reference
5. Base level"S" is a virtual flat surface calculated at three points(A10,L1,L10) of back side terminal
6. The center of the effective image area relative to "B" and "B'" is (H, V) = (6.40, 5.80) ± 0.075 mm
7. The rotation angle of the effective image area relative to "H" and "V" is ± 0.5°
8. The height from the bottom "C" to the effective image area is 0.92 ± 0.1 mm
9. The tilt of the effective image area relative to the bottom "C" is less than 0.05 mm
10. The tilt of the effective image area relative to the bottom "D" of the cover glass is less than 0.05 mm
11. The thickness of the cover glass is 0.50 mm, and the refractive index is 1.5
12. The seal overflows is up to the maximum size of the package
13. Below letter is appropriate in "W" ~ "Z". (No Au coat)
    W : English Capital letter, single letter. X : Number, single letter.
    Y : Number, single letter. Z : Number, single letter.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT	0.7g
DRAWING NUMBER	AS-C83(E)